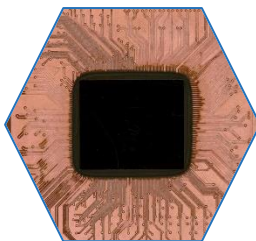
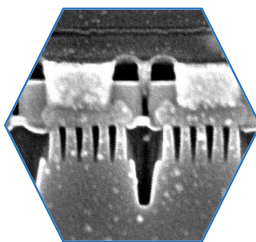


Ambarella CV2 Computer Vision SoC

Ambarella vision processor using Samsung's 10nm process targeting video surveillance, home security camera and machine vision applications.



Title: Ambarella CV2 Computer Vision SoC

Pages: 119

Date: August 2021

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Price: EUR 3,990

Reference: SPR21638

Ambarella is one of the leading developers of low-power and ultra high-definition video processing processors. Ambarella introduced the CV2 with full System on Chip (SoC) functionality using Samsung's 10nm technology process. The CV2 SoC combines advanced computer vision, video encoding, image processing and stereo vision on a single chip.

This second generation computer vision product has improved performance with up to 20 times better processing performance compared to the first-generation CV1 processor. The CV2 processor consumes little power, and the computer vision architecture enables object recognition with high accuracy.

Significant die area is devoted to the stereo image processor, the Image Signal Processor (ISP), and the video codec. The quad core Arm processor with L2 cache occupies a relatively small area compared to other circuit blocks. The main functional areas take up approximately 66% of the active area of the die.

A full teardown has been conducted to provide insights into the Ambarella CV2 Computer Vision SoC, which is integrated in Hanwha Technwin's Wisenet Network Camera. To reveal all the details of Ambarella's SoC, this report features multiple analyses including a floor plan

analysis to understand the high-level chip architecture with Intellectual Property (IP) block area contribution measurements. It identifies all the chip features and Samsung's 10nm process. The report includes package and CV2 die cross section and the back-end construction analysis for packaging structure.

The complete process is built from 3D X-Ray images, optical, SEM cross-sections, material analysis and delayering. This report includes detailed manufacturing process and an estimation of the wafer, die and component cost.

COMPLETE TEARDOWN WITH

- Detailed photos
- Precise measurements
- Materials analysis
- Floor plan analysis
- 3D X-ray images
- Manufacturing process flow
- Supply chain evaluation
- Manufacturing cost analysis

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Selling Price

AUTHORS



Belinda Dube is working for System Plus Consulting as an Engineer & Analyst, Semiconductor Memories. Belinda is also engaged in the development of reverse engineering & costing analyses with the power electronics and compound semiconductors team.



Don Scansen has partnered with System Plus Consulting to launch the new die architecture and front-end process analysis of advanced SoC devices including APU, CPU, GPU, and FPGA. Don previously supported clients ranging from individual patent owners to Fortune 500 companies providing competitive analysis and intellectual property support. He holds a PhD in electrical engineering.



Véronique Le Troadec has joined System Plus Consulting as a laboratory engineer. Coming from Atmel Nantes, she has extensive knowledge in failure analysis of components and in deprocessing of integrated circuits.

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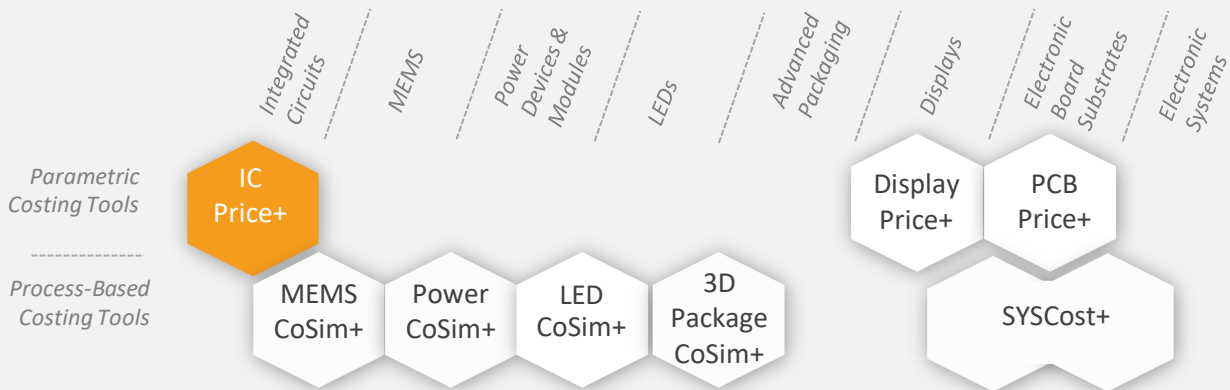
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