Apple M1 System-on-Chip

The Apple’s first ARM based processor for Personal Computing

SP20608 - IC report by Belinda Dube, Stéphane Elisabeth and Don Scansen
Physical analysis by Véronique Le Troadec and Don Scansen

December 2020 – Sample
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Executive Summary

This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the **Apple M1 System-on-Chip (SoC)**.

Back in 2010, Apple managed to get ride of Samsung’s Processor to use its own developed ARM core-based processor, the A4. Still produced by Samsung, this was the first of the series to integrate an ARM Cortex-A8 in the iPhone Series. Still developing its own processor, Apple is now supplying the processor from TSMC since 2014. Now coupled with its packaging services including integrated Fan-Out (iFO) technology, TSMC is the only processor supplier for Apple.

Two new Apple MacBook models and the Mac mini are now powered by an Apple in-house System-on-Chip (SoC) design: the M1. The transition from Intel x86 processors has created shockwaves felt throughout the processor and computing world. This new, first SoC for Mac features 4-CPU high-performance cores, 4-CPU high-efficiency cores, and 8-GPU cores. The tight software-hardware integration inside Apple enabled a compact, efficient processor for personal computer that outcompetes many premium microprocessors. 16 billion transistors using TSMC 5nm process were used to build it.

On the SoC side, it appears that the die area of the M1 was optimized for functionality rather than SRAM cache. There is limited on-chip cache, taking cues from mobile SoC designs relying on the universal memory architecture (UMA) concept and external LPDDR4X DRAM. Significant die area is devoted to standard cell functions, indicating that Apple is leveraging in-house chip design to optimize hardware for the operating system. On the packaging side, the same structure is used for Apple’s A12X and A12Z, with the integration of the DRAM on the SoC substrate, and embedded silicon capacitors in the substrate.

To reveal all the details of this new, exceptional SoC, this report features multiple analyses: a floor plan analysis to understand the high-level chip architecture with IP block area contribution measurements, a front-end construction analysis that reveals the most interesting features of the new TSMC 5nm process, a back-end construction analysis of the packaging structure, and a detailed manufacturing cost analysis. Along with a complete construction analysis using SEM cross-sectional materials analyses, and delayering, the front-end analysis employs a high-resolution TEM cross-section to expose the high-mobility channel of the 5nm process, and the back-end analysis uses CT-Scan (3D X-ray) to reveal the layout structure of the package.
Executive Summary – Floor Plan Analysis

This floorplan analysis of the Apple M1 system-on-chip is intended to provide critical insights into the chip architecture. The M1 is the first Apple in-house design for deployment to their personal computer line after many years and iterations of the mobile AX products (most recently A14).

Confirming the Apple marketing material, the M1 SoC contains these major IP blocks:

- Four “Firestorm” high-performance CPU cores
- Four “Icestorm” power efficient CPU cores
- Eight GPU cores
- Machine learning core – “Neural Engine”
- Dual core secure processor – “Secure Enclave”
- PCI Express high speed serial interfaces (X2)
- Display engine

Taking many queues from the mobile architecture, the M1 limits on-chip SRAM to a great extent. The total of L2 SRAM arrays is estimated to be 27.8 MB. The unified memory architecture (UMA) allows sharing of the LPDDR4X DRAM between the monolithic CPU and GPU cores. The incorporation of the DRAM on a common BGA substrate with the M1 silicon is similar in concept to typical mobile application processors (APU). However, the APU for mobile products typically deploys the LPDDR variant in a package-on-package configuration over the APU. The M1 package is more suited to higher performance and higher power consumption applications such as desktops and laptops since heat sinks can be directly applied to the M1 SoC.
Apple Mac Mini Overview

Overview / Introduction

Company Profile & Supply Chain

Physical Analysis
- Apple Mac Mini Teardown
  - Apple M1 Package Analysis
    - Views & Dimension
    - Package X-RAY
    - Package Opening
    - Cross Section 1
    - Cross Section 2
    - M1 Package Process
  - DRAM
    - Package Views
    - Package X-RAY
    - Package Cross Section
    - Package Opening
    - Die Views
    - Die Cross Section
  - M1 SoC Die
    - Die Views
    - Die Marking
    - Die Delayering
    - Die Cross Section

Floor Plan
- FEOL (TEM Analysis)
- Manufacturing Process Flow
- Cost Analysis
- Related reports
- About System Plus

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Apple Mac Mini TearDown

**Physical Analysis**
- Apple Mac Mini Teardown
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    - Die Cross Section

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**Apple Mac Mini Board Heatsink** ©2020 by System Plus Consulting

Material

Material Removal

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There are different types of TIM used on the DRAM and on the IHS.

The **[formula] maximizes**
PHYSICAL ANALYSIS
Packaging
M1 Package Views & Dimensions

- **M1 Package**:
  - SiP BGA
  - **Ball Pitch**: mm
  - **Dimensions**: mm

- **DRAM Package**
  - **Dimensions**: mm

- **IHS Package**
  - **Dimensions**: mm
M1 FLI Map

Key Attributes

<table>
<thead>
<tr>
<th>Feature</th>
<th>Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Foundry</td>
<td>Min FLI Pitch, μm</td>
<td></td>
</tr>
<tr>
<td>Process node</td>
<td>nm</td>
<td></td>
</tr>
<tr>
<td>Metal Layers</td>
<td>Die Area, mm²</td>
<td></td>
</tr>
</tbody>
</table>

Physical Analysis
- Apple Mac Mini Teardown
- Apple M1 Package Analysis
  - Views & Dimension
    - Package X-RAY
    - Package Opening
  - Cross Section 1
  - Cross Section 2
  - M1 Package Process
- DRAM
  - Package Views
  - Package X-RAY
  - Package Cross Section
  - Package Opening
  - Die Views
  - Die Cross Section
- M1 SoC Die
  - Die Views
  - Die Marking
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  - Die Cross Section

FloorPlan
FEOL (TEM Analysis)
Manufacturing Process Flow
Cost Analysis
Related reports
About System Plus
The capacitors are placed on the M1 SoC Package PCB face down, the capacitors are connected to the PCB using microbumps.

- Capacitor thickness: \( \mu \text{m} \)
- The capacitor Die process uses metal layers.
M1 Package Cross Section 2 - Package PCB

- **Trench thickness:** $\mu$m
- **Si is etched to form a deep trench. Polysilicon is deposited and a dielectric layer is deposited between two polysilicon materials.**
- **Dielectric layer:** $\text{nm}$
- **The capacitor process uses polysilicon layers.**
- Distance between DRAM Package and M1 Die: \( \text{mm} \)
- M1 SoC Die distance to PCB edge: \( \text{mm} \)
Package Cross Section – Summary

- DRAM Package Cross Section
- M1 SoC Package Cross Section
- M1 SoC Package – metal cover Removal

- DRAM Package Balls
  - M1 Package PCB Ball pitch: \( \mu \text{m} \)
  - Ball Diameter: \( \mu \text{m} \)

- M1 SoC Package Balls
  - M1 Package PCB Ball pitch: \( \mu \text{m} \)
  - Ball Diameter: \( \mu \text{m} \)

- Capacitor
  - Capacitor microbump Pitch: 4 \( \mu \text{m} \)
  - Microbump Diameter: 2 \( \mu \text{m} \)

- M1 SoC Microbumps
  - M1 Die Microbump Pitch: \( \mu \text{m} \)
  - Microbump Diameter: \( \mu \text{m} \)
DRAM memory cross-section reveals:

- Transistors
- Metal contacts and metal layers

- The memory process uses Cu metal layer and a thick Aluminium metal pad
- The memory process uses 5 metal layers: 3 Cu + 2 Al
Type: SRAM 6 transistors

Cell size:

- \( \mu m^2 \)
- \( \mu m \times 0.09 \mu m \)
- This corresponds to TSMC’s \( \text{nm} \) technology node
M1 SoC Die - Cross Section

- M1 Die thickness: \( \mu m \)
- The M1 SoC Die is placed in flip chip position on the PCB substrate.
• The Processor Die uses metal layers (Cu + Al)
Die Floorplan – Major IP Block Area Utilization

<table>
<thead>
<tr>
<th>IP Block</th>
<th>Area (mm²)</th>
<th>% of Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Performance Compute Complex (4 Core HP CPU + 12MB L2 cache, Firestorm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency Compute Complex (4 Core Eff. CPU + 4MB L2 cache, Icestorm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 Core GPU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 Core Neural Engine</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 mB Shared SRAM Cache</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Core Secure Enclave</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standard Cell Logic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LPDDR4X Interface Total (CH 1–8)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual Core ISP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Display Engine</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCI Express (Lane 1 + Lane 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HS I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other Serial I/O (2 Blocks)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Major IP Block Area Summary with Percentage Die Contributions

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Die Floorplan – Detail of Constituent Circuit Blocks

<table>
<thead>
<tr>
<th>Constituent Block (Not Comprehensive)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP CPU Core, Firestorm (B1 + C1 block)</td>
<td></td>
</tr>
<tr>
<td>Efficient CPU Core, Icestorm (D1 block)</td>
<td></td>
</tr>
<tr>
<td>GPU Core (A1 block)</td>
<td></td>
</tr>
<tr>
<td>Neural Engine Core</td>
<td></td>
</tr>
<tr>
<td>8 mB Shared SRAM Cache (blocks SS6–8)</td>
<td></td>
</tr>
<tr>
<td>Secure Enclave Core (F1 block)</td>
<td></td>
</tr>
<tr>
<td>LPDDR4X Interface (Block LP1)</td>
<td></td>
</tr>
<tr>
<td>HP CPU L2 SRAM Cache Array (block SS1)</td>
<td></td>
</tr>
<tr>
<td>HP CPU L2 SRAM Cache Array (block SS2)</td>
<td></td>
</tr>
<tr>
<td>HP CPU L2 SRAM Cache Array (block SS3)</td>
<td></td>
</tr>
<tr>
<td>HP CPU L2 SRAM Cache Array (block SS4)</td>
<td></td>
</tr>
<tr>
<td>Efficient CPU L2 SRAM Cache Array (block SS9)</td>
<td></td>
</tr>
</tbody>
</table>

Note: Area annotations on image rounded to ± 0.1mm²
The engineered high mobility channel (HMC) employed in the PMOS finFET of the nm process is indicated by the darker band of contrast in the bright field (BF) TEM image at right.

- This darker band is a region of material.
- Its position on the fin is near the bottom of the active channel where the metal gates overlap it but do not extend much beyond it.
- The layer is approximately nm thick and begins nm below the top of the fin.
FEOL Analysis – TEM Along PMOS Fin

The Ge signal near the top of the fin (at base of metal contact) is thereby performance of the p-type channel.

Upper portions of the active fin channel appear to have lower

Epitaxial region of active fin channel

The silicon.

Detail of PMOS FinFET with EDS Materials Analysis of the Fin Composition by 2D Mapping of the Characteristic X-rays

©2020 by System Plus Consulting
The lower fin is Si (below the etch back).

The first epitaxial region in the lower part of the PMOS fin.

As epitaxy continues to grow.

The compressive stress boosts the...
MANUFACTURING PROCESS FLOW
Packaging Process Flow (2/4)

**PCB Substrate**
- Resin Lamination
- Die Pick and Place Deposition
- Resin Lamination
- Hot Press
- Electroless copper plating
- Laser Drilling

Copper seed
C O S T
ANALYSIS
### M1 SoC Wafer & Die Cost

<table>
<thead>
<tr>
<th></th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Front-End Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BE: Bumping Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BE: Probe Test Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BE: Backgrindng &amp; Dicing Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total Wafer Cost</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nb of potential dies per wafer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nb of good dies per wafer</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Front-End Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BE: Bumping Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BE: Probe Test Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BE: Backgrindng &amp; Dicing Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BE: Yield losses</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Die Cost</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

By adding the bumping cost, probe test cost, the thinning and the dicing cost, the wafer cost is estimated at $\_\_\_\_\_\_ in low yield and $\_\_\_\_\_\_ in high yield.

The number of good dies per wafer is estimated at $\_\_\_\_\_\_ in low yield and $\_\_\_\_\_\_ in high yield, which results in a die ranging from $\_\_\_\_\_\_ in low yield and $\_\_\_\_\_\_ in high yield.
DRAM Memory - CMOS and Top Metal Layers Front-End Cost

This front-end cost includes STI insulation, 3 Bottom metal layers (word line in Tungsten, bit line in Tungsten, bit line contacts), CMOS transistors and 5 top metal layers.

The CMOS transistors, 3 bottom and 5 top metal layers front-end cost is **between high and medium yield**.

The largest portion of the manufacturing cost is due to the **equipment cost** at **Cost Comparison**.
The DRAM 4GB/32Gb component cost ranges from $5 to $15 according to yield variations.

- The **memory dies** represent 50% of the component cost.
- The **packaging** represents 25% of the component cost.
- **Final test and yield losses** account for 25% of the component cost.

(4GB/32Gb) LPDDR4 DRAM Memory market price is estimated to be between $5 and $10 in Q1 2021.
### Embedded Die Packaging Cost

<table>
<thead>
<tr>
<th>Embedded Die Package</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
<td>Breakdown</td>
</tr>
<tr>
<td>Embedding Process</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HDI Process</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outer Layer Process</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Module Fab Test</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Automation Scrap</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Embedded Die Process Cost per Panel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No Modules per Panel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Embedded Die Process Cost per Module</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OSAT Gross Profit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Embedded Die Process Price per Module</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The **embedded die package cost per panel** ranges from $X$ to $Y$ between low and high yield (panel size of **335mm x 340mm**).

- The number of modules per panel is estimated to be **X** between low and high yields.
- This results in **embedded die process cost per module** ranging from **X** to **Y** between low and high yields.
- We estimate a **%** gross margin for the OSAT.
- The **embedded die process price per module** is estimated at **X** in low yields and **Y** in high yields.
## Embedded Die Packaging Steps Cost

<table>
<thead>
<tr>
<th>Process</th>
<th>Cost Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDI Process - CO2 laser desmear</td>
<td>0.35%</td>
</tr>
<tr>
<td>HDI Process - Laser drilling 40µm</td>
<td>0.20%</td>
</tr>
<tr>
<td>HDI Process - CO2 laser desmear</td>
<td>0.15%</td>
</tr>
<tr>
<td>HDI Process - Cu electroless plating 1µm</td>
<td>0.14%</td>
</tr>
<tr>
<td>HDI Process - Photoresist Deposition</td>
<td>0.13%</td>
</tr>
<tr>
<td>HDI Process - Photoresist exposure</td>
<td>0.12%</td>
</tr>
<tr>
<td>HDI Process - Photoresist Developing</td>
<td>0.11%</td>
</tr>
<tr>
<td>HDI Process - Cu electroplating</td>
<td>0.10%</td>
</tr>
<tr>
<td>HDI Process - Photoresist stripping</td>
<td>0.09%</td>
</tr>
<tr>
<td>HDI Process - Copper Etching</td>
<td>0.08%</td>
</tr>
<tr>
<td>HDI Process - Cleaning</td>
<td>0.07%</td>
</tr>
<tr>
<td>HDI Process - AOI Inspection</td>
<td>0.06%</td>
</tr>
<tr>
<td>HDI Process - Lamination Preparation</td>
<td>0.05%</td>
</tr>
<tr>
<td>HDI Process - Resin lamination</td>
<td>0.04%</td>
</tr>
<tr>
<td>HDI Process - Dicing the edges</td>
<td>0.03%</td>
</tr>
<tr>
<td>HDI Process - Cleaning</td>
<td>0.02%</td>
</tr>
<tr>
<td>HDI Process - Thickness control</td>
<td>0.01%</td>
</tr>
<tr>
<td>HDI Process - Laser drilling 50µm</td>
<td>0.00%</td>
</tr>
<tr>
<td>HDI Process - CO2 laser desmear</td>
<td>0.00%</td>
</tr>
<tr>
<td>HDI Process - Laser drilling 50µm</td>
<td>0.00%</td>
</tr>
<tr>
<td>HDI Process - Cu electroless plating 1µm</td>
<td>0.00%</td>
</tr>
<tr>
<td>HDI Process - Photoresist Deposition</td>
<td>0.00%</td>
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<tr>
<td>HDI Process - Cu electroplating</td>
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</tr>
<tr>
<td>HDI Process - Photoresist stripping</td>
<td>0.00%</td>
</tr>
<tr>
<td>HDI Process - Copper Etching</td>
<td>0.00%</td>
</tr>
</tbody>
</table>

**Total Cost:** 100%
Related Reports

**REVERSE COSTING ANALYSES - SYSTEM PLUS CONSULTING**

Power & IC
- Intel Foveros 3D Packaging Technology
- Advanced System-in-Package Technology in Apple’s AirPods Pro
- Nvidia Tegra K1 Visual Computing Module

**MARKET AND TECHNOLOGY ANALYSES - YOLE DÉVELOPPEMENT**

- Processor Quarterly Market Monitor
- Status of the Advanced Packaging Industry 2020
- Fan-Out Packaging Technologies and Market 2020
Business Models a Fields of Expertise

- Custom Analyses (>130 analyses per year)
- Reports (>60 reports per year)
- Costing Tools
- Trainings

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Manufacturing Process Flow
Cost Analysis
Selling Price Analysis
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