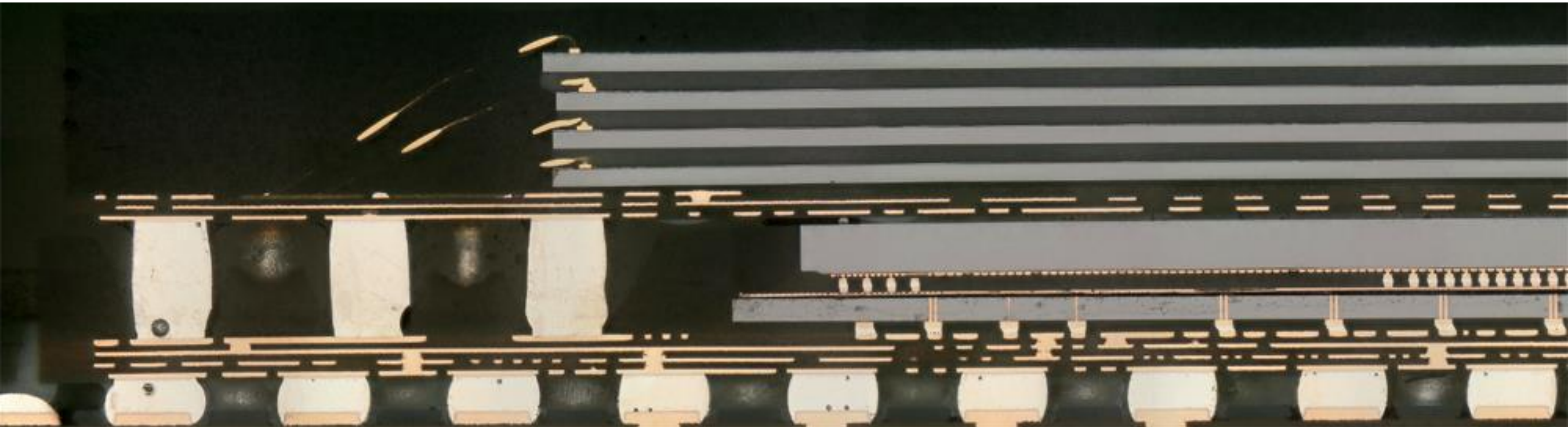
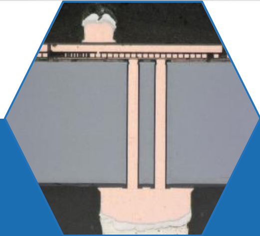
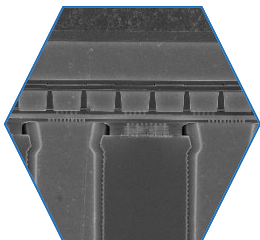
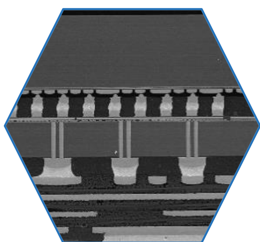


Intel Foveros 3D Packaging Technology

Intel Core i5-L16G7: the first utilisation of Intel's Foveros Technology with Package-on-Package configuration in a consumer product.







Title: Intel Foveros 3D packaging technology

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As feature scaling hits the limits of physics, the semiconductor industry is already researching for "more-than-Moore" technology enablers. In this area, multi-die packages are essential to integrate more functions into a small form factor, whatever is the lithographic technology node. All this must be at low cost and in a short time to market. From this perspective, Intel has developed several interconnect technologies to enable heterogenous integration using chiplets. An early glimpse of the technology enablers was seen in 2018 on an Intel processor, then called Embedded Multi-die interconnect Bridge (EMiB). Today, Intel shows another way to interconnect dies in processor using an active interposer and Foveros technology.

Foveros allows 3D Face-to-Face (F-F) stacking for integration of different types of devices on an active interposer using Through Silicon Vias (TSVs). The interposer is used as a bridge for the different chiplets. However, it also comprises low-power components such as input/output (I/O) connections and power delivery with high performance logic.

The Intel Core i5-L16G7 analyzed in this report features Intel's hybrid packaging technology. This technology relies on Foveros F-F die stacking and Package-on-Package (PoP) configuration. The design aims to integrate 10 nm computing die with SK Hynix LPDDR4 DRAM in a PoP architecture in a single package. This lowers power consumption and increases core performance while reducing the form factor and z-height to fit ultra-mobile applications.

This report constitutes an exhaustive analysis of the Intel Core i5-L16G7 processor. This report includes a full investigation of Intel's hybrid packaging technology. It features a detailed study of the 3D package including the processor die, Foveros features and interposer die analysis and cross-sections. The report also integrates the physical analysis of the LPDDR4X DRAM dies integrated in the package. Finally, it contains a complete cost analysis and a selling price estimation of the component and a physical comparison with TSMC's Chip-on-Wafer-on-Substrate (CoWoS) technology.

COMPLETE TEARDOWN WITH

- Detailed photos
- Precise measurements
- Material analysis
- Manufacturing process flow
- Supply-chain evaluation
- Manufacturing cost analysis
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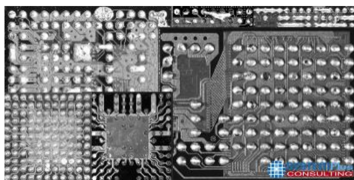

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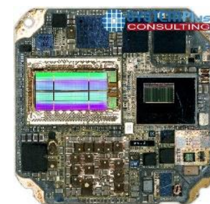

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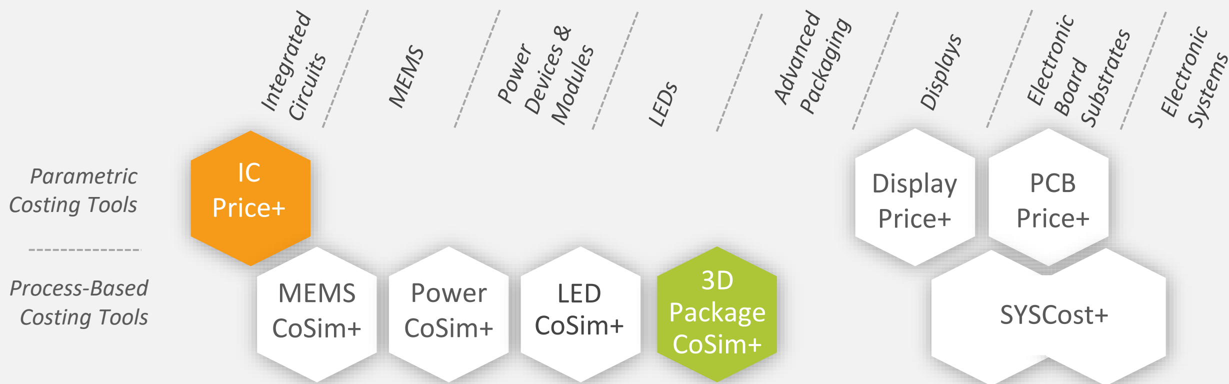

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