Advanced System-in-Package Technology in the Apple AirPods Pro

Packaging report by Belinda DUBE
Laboratory Analysis by Youssef EL GMILI
March 2020 – SAMPLE
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Executive Summary

This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the AirPods Pro SiP Audio System. The full system includes two SiP modules and 2 MEMS modules.

System-in-Package (SiP) market attained a huge revenue of $13.4 billion in 2019 and is expected to achieve approximately $18.8 billion is 2025. The market is mainly driven by increased need for advanced architectures in electronic devices mostly in mobile and consumer products. Advanced technology asks for higher levels of die and functionality integration in a single package at lower cost. Since 2015, Apple has integrated several generations of SiP in its Smartwatch. This year, for the first time, the company has chosen the same type of solution for its earbuds. This came in two different SiP, one for the Bluetooth connectivity and one for the audio codec.

Apple’s AirPods adopt SiP for the first time in the latest AirPods Pro. The SiP influences device compactness and size reduction of the wireless headsets. The AirPods Pro designed and manufactured by Apple comprises of several SiPs assembled together: Two Inertial Measurement units (IMU), one Bluetooth Module and one Audio Codec Module. The IMUs are standard LGA SiPs from STMicroelectronics.

The Bluetooth Module called H1-Module is packaged using double side Molding technology in order to integrate a memory under the System-on-Chip (SoC). This structure enables wireless connection, drives voice enabled Siri and enforces real time noise cancellation. The Audio Codec integrated up to 8 dies and 80 passives components with a density of 0.96 components per mm².

The module has a special shape that is designed to be mechanically constraint in the earbuds to maximize the lost area in the system. Both SiP are designed in order to has better power management, higher performances with a high cost effectiveness.

The report includes all the packaging details from the substrate to the dies from both SiP modules. The report focuses on the packaging processes of the two SiP modules and the final assembly. High Resolution Images of the Package Cross Section at different positions and angles enables a full package and assembly process analysis. It also includes a full description of the process and the manufacturing cost of the dies and the packaging. Finally, a physical comparison of the two SiP Modules is included.
Executive Summary

The reverse costing analysis is conducted in 3 phases:

Teardown analysis

- Package is analyzed and measured,
- The dies are extracted in order to get overall data: dimensions, main blocks, pad number and pin out, die marking,
- Setup of the manufacturing process.

Costing analysis

- Setup of the manufacturing environment,
- Cost simulation of the process steps.

Selling price analysis

- Supply chain analysis,
- Analysis of the selling price.
Apple AirPods Pro Earbuds

Microphone
External noise detection
An inward microphone inside the ear.

SiP H1 Module
SiP Audio Codec Module

Apple AirPods and Audio Module ©Apple

AirPods Pro Right Earbud – View
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AirPods Pro TearDown

Physical Analysis
- Global Overview
- AirPods Pro TearDown
- Full Audio Module System
  - View & Dimensions
  - X-Ray View
  - Module Opening
- Audio Code Module
  - Opening & Cross-Section
  - Audio Code - Die 1
  - Operation Amplifier - Die 2
  - Audio Amplifier - Die 3
  - Touch Controller - Die 4
  - LED Driver - Die 5
  - Circuit Regulator - Die 6
- Bluetooth Module/ H1 Module
  - Overview
  - Memory Die - Die X
  - H1 Processor - Die 1
  - RF Circuit - Die 2
- MEMS Modules
  - STMicro MEMS Module
  - Bosch MEMS Module

Physical Comparison

Manufacturing Process Flow

Cost Analysis

Feedbacks

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Module X-Ray View

- X-Ray images reveal the integrated in the Module.
- The dies occupy approximately % of the Top Module package surface area.
- The X-Ray image reveals the integrated in the Module.
Module Cross-Section

- Cross-section of the package reveals the die placement on the Top Module PCB and the Bottom Module PCB.
- The Top Module PCB is attached to the Bottom Module/H1 Module PCB using Package Conformal shielding structure is also revealed covering the whole Top module and the Bottom H1 Module.
- A die is placed between the Top Module PCB and Bottom Module PCB.
Top Module  Audio Code – Cross-Section

- The package Cross-Section reveals the layout and configuration on PCBs.
- Die 1 Audio Code is placed on the top module.
Top Module Operation Amplifier - Cross-Section

- connect the Operation Amplifier Die 2 to the PCB.

- The ___ layer is deposited and patterned. A thin seed layer of ___ is deposited and polymer layer is deposited and patterned to create opening for the copper redistribution layer.

- The ___ layer is electroplated.

- A ___ layer is deposited and patterned and copper ___ is deposited.
Top Module Circuit Regulator - Die 6 Cross Section

- The Cross-Section reveals the passive components and Die 6, the Circuit Regulator.
• The circuit regulator die has a copper interconnect layer to ensure connection of the PCB and die metal layers.
• A layer under the bump is deposited and patterned.
• A layer is deposited and patterned. This layer is between the solder ball and the PCB copper metal.
Bottom Module Memory Die - Cross-Section

- Memory Die is deposited on the PCB.
- The die attaches to the memory die to the PCB.
Module Cross-Section - MEMS Modules

- The Bottom Side has two Sensor Modules integrated on a different PCB.
  - MEMS Module: Accelerometer and Gyroscope
  - Module: Accelerometer
Top Module Die 1 - WLSCP

Die Wafer
- The wafer is cleaned
- Lamination of foil into carrier

Die Wafer
- Place wafer on top of wafer upside down
- Wafer is thinned and Cover Molding is deposited.
- The die is then flipped

Die Wafer

Die Wafer
- Electroplate UBM
- Etch silicon material and pattern
- Ball Drop and dice
- Attach to PCB
### H1 Die - Wafer Front-End Cost

<table>
<thead>
<tr>
<th>Front-End</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Raw wafer Cost 300mm</td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Equipment Cost</td>
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<tr>
<td>Consumable Cost</td>
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<td></td>
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<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield losses Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>H1 Processor Front-End Cost</strong></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Foundry Gross Profit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mask Set Depreciation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>H1 Processor Front-End Price</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The **front-end cost** for the die circuit is estimated between $ and $ according to yield.

The largest portion of the manufacturing cost is due to the

We estimate a **gross margin of** $% for the die supplier and mask set depreciation, which result in a **Wafer price** at $ in 2020 and $.
Top Module - Audio Codec Module Packaging Cost

### Table: Total Cost of Dies and Passive Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio Code Die Price</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operation Amplifier Die Price</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Audio Amplifier Die Price</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Touch Controller Die Price</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LED Driver Die Price</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Circuit Regulator Die Price</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Passive Components Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total Cost</strong></td>
<td>1,500</td>
<td>2,500</td>
<td>3,500</td>
</tr>
</tbody>
</table>

### Table: Bottom SiP Module Assembly

<table>
<thead>
<tr>
<th>Component</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Substrate Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable Cost</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield Losses Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Package Manufacturing Cost</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OSAT Gross Profit</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The **Total Cost of Dies and Passive components** is estimated at **$3,000**.

The **Package Manufacturing Cost** is estimated between **$500** and **$1,000**.

We estimate a gross margin of 16% for the die packaging, which result in packaging price between **$50** and **$100**.

The largest portion of the manufacturing cost is due to the **materials**.
Audio Codec Module - Packaging cost per process steps

### Packaging Total Cost Per Step

<table>
<thead>
<tr>
<th>Process Operation</th>
<th>TOTAL COST (USD / Unit)</th>
<th>Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measurement Multi-Steps</td>
<td>0.4%</td>
<td></td>
</tr>
<tr>
<td>Cleaning Multi-Steps</td>
<td>4.8%</td>
<td></td>
</tr>
<tr>
<td>PCB Substrate - Pick &amp; Place</td>
<td>1.4%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5.0%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>16.2%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.7%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.4%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.0%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.4%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.8%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.0%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>52.0%</td>
<td></td>
</tr>
<tr>
<td>Package Marking - Laser Mark</td>
<td>0.7%</td>
<td></td>
</tr>
<tr>
<td>Package - Dicing - Mechanical Saw</td>
<td>0.1%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.4%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.3%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.2%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.3%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.3%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.9%</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>$3</strong></td>
<td><strong>100.0%</strong></td>
</tr>
</tbody>
</table>
The total **panel cost** ranges from $\text{Low Yield}$ to $\text{High Yield}$ according to yield variations.

The number of **good packages per wafer/panel** is estimated at $\text{Low Yield}$ which results in a **die cost** ranging from $\text{Low Yield}$ to $\text{High Yield}$.
Module Assembly Cost

The package manufacturing cost is estimated between

The largest portion of the manufacturing cost is due to the

We estimate the packaging gross margin of , this results at the packaging price varying from

<table>
<thead>
<tr>
<th>Package Manufacturing Cost Breakdown (Medium Yield)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Image of a pie chart showing cost breakdown]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Top Module</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bottom H1 Module</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ST Microelectronics MEMS Module</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Bosch MEMS Module</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Passive Components &amp; Antenna</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-Layer Added PCB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dies per Reconstruct Panel</th>
<th>Reconstituted Wafer Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Image of cost breakdown table]</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Final Module Assembly</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clean Room Cost</td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
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<tr>
<td>Equipment Cost</td>
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<tr>
<td>OSAT Gross Profit</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Package Manufacturing Price</td>
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</table>

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