Back in 2015, only Outsourced Semiconductor Assembly and Test (OSAT) players were involved in Fan-Out (FO) packaging. In 2016, TSMC led the entry of foundries into this market with its integrated FO (inFO) packaging technology. Next, Integrated Device Manufacturers (IDMs) like Samsung joined the race with new in-house technology at the panel level. The result is that in 2019 OSATs have only a third of the market. Even with this reduced share, they are still developing and enhancing their portfolio in this segment. Recently ASE, in partnership with Deca Technologies, has entered the core market with its M-Series technology. Next, nepes bought the technology from Deca. As the market is continuously moving, System Plus Consulting offers an overview of the technologies on the market, providing the original equipment manufacturers’ (OEMs') technical and cost choices of fan-out packaging.

This report provides insights on technology data for FO packaging for different application segments. It includes a comparative study of eight components from power management integrated circuits (PMICs) to processors to radar Monolithic Microwave Integrated Circuits (MMICs) using Fan-Out technology from different suppliers.

Physical data of several components has been compared in term of process flow, cost and integration to provide a large panel of OEM technical and economic choices from the market such as:

- embedded Wafer Level Ball (eWLB) grid array from Infineon, Amkor and STATSChipPAC
- Redistributed Chip Package (RCP) from nepes
- M-Series from ASE/Deca Technologies
- Integrated Fan-Out (inFO) from TSMC
- Enhanced Panel Level Packaging (ePLP) from SEMCO

The report includes a description of each process flow for the five major fan-out technologies on the market. It also contains a complete cost analysis of the packaging and tries to explain OEM choices.

**COMPLETE TEARDOWN WITH**

- Comparative study with photos and cross-sections
- Precise measurements: line/space, materials, dimensions
- Manufacturing process flow
- Supply chain evaluation
- Manufacturing cost analysis
- Cost comparison
### Overview/Introduction

**Fan-Out Technologies:**
- Infineon’s eWLB
- neps’ RCP
- TSMC’s info
- Samsung’s ePLP
- ASE’s M-Series

**Device Teardown:**
- Denso Radar and Continental Radar
- Apple Watch Series 4 and Samsung Galaxy Watch
- Samsung Galaxy S10 5G and Samsung Galaxy S7 Edge
- FitBit Charge 3

**Physical Comparison: Dimensions, Materials, Structure**
- eWLB vs. RCP (Infineon RNN7745P vs. NXP MR2001) For Thermal Dissipation
- inFO vs. ePLP (A12 vs. Exynos 9110) For High I/O Density
- eWLB vs. M-Series (WCD9335 vs. PM8150) For Side Wall Protection
- RCP vs. eWLB (SCM-iMX6 vs. CY8C68237FM-BLE) For SiP
- Packaging Analysis

### Manufacturing Process Flow
- Global Overview: Thermal Dissipation, High I/O, Side Wall Protection, SiP
- Fan-Out Packaging Process & Fabrication Unit

### Cost Analysis
- Summary of the cost analysis
- Yields Explanation & Hypotheses
- Front-End Cost Analysis
- MMIC packaging for thermal dissipation Cost Analysis
- AP packaging for High I/O Cost Analysis
- Audio Codec packaging for Side Wall Protection Cost Analysis
- Packaging for SiP Cost Analysis

### Cost Comparison
- Summary of physical and cost analysis
- Board Level Reliability vs. Cost Estimation

### RELATED REPORTS

**ASE/Deca M-Series Fan-Out Process**
ASE/Deca’s patented fan-out technology has penetrated a new commercially available device, the Qualcomm PM8150 PMIC.
September 2019 - EUR 3,990*

**Advanced packaging technology in the Apple Watch Series 4’s SiP**
Four major packaging technologies: ASE’s SiP & modified SESUB, TSMC’s inFO-ePoP, Skyworks’ Double Side BGA.
January 2019 - EUR 3,990*

**Samsung Exynos 9110 with ePLP: First Generation of Samsung’s FO-PLP**
The first ultra-small multi-chip High Volume Manufacturing (HVM) FO-PLP device for consumer applications found in the Samsung Galaxy Watch.
November 2018 - EUR 3,990*

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Dr. Stéphane Elisabeth has joined System Plus Consulting’s team in 2016. He has a deep knowledge of Materials characterizations and Electronics systems. He holds an Engineering Degree in Electronics and Numerical Technology, and a PhD in Materials for Microelectronics.
Reverse Costing® is the process of disassembling a device (or a system) in order to identify its technology and calculate its manufacturing cost, using in-house models and tools.

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