3D NAND Memory Comparison 2019

Comparison of Leading Edge 3D NAND Memories

TOSHIBA-SANDISK / SAMSUNG/SK HYNIX/MICRON-INTEL

SP19483 - Memory report by Belinda Dube

December 2019 – Sample
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Executive Summary

NAND Flash memory manufacturers continue to increase word lines in order to meet the customer demands of elevated memory capacity per die and faster read and write frequencies. By increasing the worldlines manufacturers face technical challenges that could induce defects in the NAND memories. Some manufacturers have introduced a new manufacturing process to overcome the limitations of stacking.

We present detailed technological and economical comparison of latest generation of 3D NAND flash memory available on the market today from four different manufacturers. These are the 96-layer designs from Toshiba/SanDisk, and Micron, 92- layers from Samsung and the 72- layer 3D NAND by SK Hynix. We base our analysis on full teardowns of the packages and the 3D NAND dies to unveil the technology choices used by the manufacturers.

We also identify the different participants in the supply chain. These two activities allow us to simulate the cost of the memory wafers and dies.

The report contains a detailed study of the latest NAND dies. The analysis also features a detailed study of die cross section and processes. The report details the physical analysis, highlighting the cell design and memory storage type. It matches the process description with the applicable patent. The report also includes the manufacturing cost analysis and estimation of the manufacturers Gross Margin.

Finally, it features an exhaustive comparison between the studied samples, highlighting the similarities and differences and their impact on cost.
### Executive Summary

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<td>96 layer</td>
<td>TLC</td>
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<td></td>
<td>64 GB</td>
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</tbody>
</table>
## Comparison Summary

### Toshiba/SanDisk
- **Memoria** 32 GB

### Samsung
- **Memoria** 32 GB

### SK Hynix
- **Memoria** 64 GB

### Micron/Intel
- **Memoria** 64 GB

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<th>Samsung</th>
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</table>
Toshiba Memory- Package Cross Section

Adhesive between two memories: 36µm
The package contains: 2 substrates.
The BGA package contains: 18 dies

16 Memory dies +2 Dummy dies
The Dummy dies gives mechanical stability between the 4 dies.

- Capacity in 1 package: 512GB
- Capacity per Die: 32GB

Package Cross Section
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The cross section reveals Toshiba's new process of aligning the word lines.
A total of 96 lines is used to manufacture the 3D NAND Die. 96-word lines are active.
Toshiba Memory - Effective unit Area

Total NAND Cell area : \( \text{mm}^2 \)

NAND string area = \( \text{mm}^2 \)

0.85 = Shifted matrix

Total area of Unit NAND String = \( \text{mm}^2 \) strings per die.

96 layers and TLC technology = 256Gbit per die.

The memory density/die = \( \text{Gb/mm}^2 \)

Memory density in active area = \( \text{Gb/mm}^2 \)
Patent-Contact Formation

Tungsten and Copper material is used for creating drain contacts.

Applicable patents: US Application Number US 9,362,298 B2
Charge trap layer is sandwiched between semiconductor and conductive layer W

WANOS

- **W** is a high k dielectric material that improves and reduces saturation.

- Word line made of **W** have improved gate

**Manufacturing Process Flow**

**Cost Analysis**

**Cost Analysis Comparison**

**Selling Price Analysis**

**Related Reports**

**About System Plus**
Staircase etching:
Pattening of the stairs is performed **6 times**.

This technique uses 1 pattern to etch out **staircase steps**.

- Patterning is done and repeated 4 times ($4 \times 8$). This allows **Word Line layers** to be exposed.
- Each staircase contains 4 layers of silicon nitride and layers of silicon oxide.
- Another pattern is implemented to expose different word lines on different sides.
- A last pattern/etch is used to etch in the y direction to double the number of layers to pass over.
Overview / Introduction

Company Profile

Technology and market

Physical Analysis
- Physical Methodology
  - Toshiba/SanDisk
    - Synthesis
    - Package
    - Physical Analysis
    - Patent
    - Outline
  - Samsung
    - Synthesis
    - Package
    - Physical Analysis
    - Patent
    - Outline
  - SK Hynix
    - Synthesis
    - Package
    - Physical Analysis
    - Patent
    - Outline
  - Intel/Micron
    - Synthesis
    - Package
    - Physical Analysis
    - Patent
    - Outline
- Comparison

Manufacturing Process Flow
Cost Analysis
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Related Reports
About System Plus

SK Hynix Memory - Wire Bonding

Inside the Package: 8 memory dies.

Total Number of interconnect wires: 8 dies
Inteconnect wires per die: 2

Wire Diameter: ~ 2 μm

Wire Material: 

PACKAGE OPENING TOP VIEW

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SK Hynix Memory - Effective unit Area

- Each row of channel holes is shifted to optimize the channel hole density.

![Channel hole diagram](image)

Total NAND Cell area: \( \text{mm}^2 \)

Area of 4 strings =

Area of one string =

(This calculated area takes account of the slit hole area).

72 layers and TLC technology give \( \text{Gb} / \text{die} \).

Memory density/die = \( \text{Gb} / \text{die} \).

The memory density in active area = \( \text{Gb/mm}^2 \).
Micron Memory - Cross Section

- Micron’s NAND process is characterized by CMOS under Array process.
- The control word line controls movement of the memory data.
- Micron builds the NAND on the wafer and manufactures the NAND on the CMOS transistors.

Manufacturing Process Flow
Cost Analysis
Cost Analysis Comparison
Selling Price Analysis
Related Reports
About System Plus
Micron Memory - Effective unit Area

Total NAND Cell area: 348 mm²

NAND string area = 348 mm²
(This calculated area takes account of the slit hole area).

- Total number of NAND strings =
- Total number of bits in die = 256Gb/die

96 layers and TLC give 64GB per die:
- Memory density in a die = 64 GB/mm²
- Memory density in a die = 64 GB/mm²
## Die comparison

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<tr>
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<th>Samsung</th>
<th>SK Hynix</th>
<th>Micron/Intel</th>
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</thead>
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<tr>
<td><strong>Die size</strong></td>
<td><img src="image1" alt="Die size" /></td>
<td><img src="image2" alt="Die size" /></td>
<td><img src="image3" alt="Die size" /></td>
<td><img src="image4" alt="Die size" /></td>
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<tr>
<td><strong>NAND Active Area</strong></td>
<td><img src="image5" alt="NAND Active Area" /></td>
<td><img src="image6" alt="NAND Active Area" /></td>
<td><img src="image7" alt="NAND Active Area" /></td>
<td><img src="image8" alt="NAND Active Area" /></td>
</tr>
<tr>
<td><strong>Memory Die</strong></td>
<td><img src="image9" alt="Memory Die" /></td>
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<td><strong>Effective Area</strong></td>
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<td><img src="image20" alt="Die capacity" /></td>
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<td><strong>Memory density/die</strong></td>
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<td><img src="image22" alt="Memory density/die" /></td>
<td><img src="image23" alt="Memory density/die" /></td>
<td><img src="image24" alt="Memory density/die" /></td>
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<tr>
<td><strong>Memory density/active area</strong></td>
<td><img src="image25" alt="Memory density/active area" /></td>
<td><img src="image26" alt="Memory density/active area" /></td>
<td><img src="image27" alt="Memory density/active area" /></td>
<td><img src="image28" alt="Memory density/active area" /></td>
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<tr>
<td><strong>PDPW/300mm wafer</strong></td>
<td><img src="image29" alt="PDPW/300mm wafer" /></td>
<td><img src="image30" alt="PDPW/300mm wafer" /></td>
<td><img src="image31" alt="PDPW/300mm wafer" /></td>
<td><img src="image32" alt="PDPW/300mm wafer" /></td>
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<tr>
<td><strong>Potential GB/wafer</strong></td>
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<td><img src="image34" alt="Potential GB/wafer" /></td>
<td><img src="image35" alt="Potential GB/wafer" /></td>
<td><img src="image36" alt="Potential GB/wafer" /></td>
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</tbody>
</table>

- Using the [3D] technology that gains more memory space by building the NAND Cells on top of the CMOS. This technique increases the NAND cell density per die.
- The single-layer NAND in the market is still competitive compared to the new generation from other manufacturers.

*PDPW = potential Dies per wafer*
Physical analysis summary - staircase

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<td>Word lines/stairstep</td>
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<td>Lithography count</td>
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Samsung Memory Process - Slit

- Patterning and High Aspect Ratio Etching is performed,
  - CVD SiO2
  - CMP

- Deposit  
  - Deposit seed layer
  - TiN
  - CVD filling (word lines)

- Lithography
- Etch
- PECVD
- PVD seed layer
- CVD
- CVD filling
- CMP
The CMOS transistor and the metal layers front-end cost is

The largest portion of the manufacturing cost is due to the
Memory 3D 96-L Structure Front-End Cost

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The **front-end cost** for the Memory is constant at [Cost]_.

The largest portion of the manufacturing cost is due to the high cost at [Cost]_.

Total Memory Front End Price includes the fabrication cost of CMOS transistor, the metal layers, the 96L memory and yield loss cost.

Total Memory Front End Cost ranges from [Cost]_ depending on the different yield loss.
### Memory Wafer & Die Cost

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#### Cost Analysis Comparison

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#### Memory Wafer Cost

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<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
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**Front-End Cost**

- BE 0: Probe Test Cost
- BE 0: Backgrinding + Dicing Cost

**Memory Wafer Cost**

- Nb of potential dies per wafer
- Nb of good dies per wafer

**Front-End Cost**

- BE 0: Probe Test & Dicing Cost
- BE 0: Yield losses

**Memory Die Cost**

By adding the probe test cost and the dicing, the **wafer cost** ranges from **according to yield variations.**

The number of **good dies per wafer** is estimated to ranges from **according to yield variations, which results in a die cost ranging from**
Wafer Cost Comparison - Medium Yield

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<th>Manufacturer</th>
<th>NAND Wafer Cost</th>
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<td>Samsung</td>
<td>$1.837.49</td>
</tr>
<tr>
<td>SK Hynix</td>
<td>$1.849.29</td>
</tr>
<tr>
<td>Micron</td>
<td>$1.849.29</td>
</tr>
</tbody>
</table>

- Toshiba: A higher cost for the wafer due to the increased metal layers and the new fab unit cost. The equipment is new and therefore contribute to the high wafer cost.
- Samsung: Has a high expensive NAND Wafer fabrication cost; this is due to the number of patterning/lithography carried out during the manufacturing process. The extensive lithography costs contribute to the final cost of a wafer.
- SK Hynix: Has the same cost range due to the increased number of worldlines deposited.

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Overview / Introduction

Company Profile

Technology and market

Physical Analysis

Manufacturing Process Flow

Cost Analysis

Cost Analysis Comparison
- Wafer Cost
- Die Cost
- CMOS
- NAND Memory Cells
- Top metallization
- NAND Cost/Gb

Selling Price Analysis

Related Reports

About System Plus

Die Cost Comparison - Medium Yield

![Die Cost Comparison Diagram](image)

Die has the lowest cost because of the small die size. More dies are produced per wafer.

Micron has the least expensive die to capacity. Building the Word lines above the CMOS/CMOS under technique from Micron helps minimize the area of the dies and increase the density significantly. Microns die has the least expensive.

Increased NAND capacity is produced by micron per wafer.

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<tr>
<td>Samsung</td>
<td></td>
</tr>
<tr>
<td>SK Hynix</td>
<td></td>
</tr>
<tr>
<td>Micron</td>
<td></td>
</tr>
</tbody>
</table>
NAND Memory Cells Cost Comparison

- NAND Memory cell cost is cheaper than the other manufacturers, the simplified

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>3D NAND Memory Cells Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toshiba</td>
<td>5000</td>
</tr>
<tr>
<td>Samsung</td>
<td>6000</td>
</tr>
<tr>
<td>SK Hynix</td>
<td>7000</td>
</tr>
<tr>
<td>Micron</td>
<td>8000</td>
</tr>
</tbody>
</table>

3D Memory Layer Cost
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Cost Analysis
Cost Analysis Comparison
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Cost per Gb Cost Comparison

<table>
<thead>
<tr>
<th>Die size GB</th>
<th>96 layers</th>
<th>92 layers</th>
<th>72 layers</th>
<th>96 layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toshiba/SanDisk</td>
<td>512GB</td>
<td>256GB</td>
<td>512GB</td>
<td>256GB</td>
</tr>
<tr>
<td>Samsung</td>
<td>256GB</td>
<td>256GB</td>
<td>512GB</td>
<td>512GB</td>
</tr>
<tr>
<td>SK Hynix</td>
<td>256GB</td>
<td>256GB</td>
<td>512GB</td>
<td>512GB</td>
</tr>
<tr>
<td>Micron</td>
<td>256GB</td>
<td>256GB</td>
<td>512GB</td>
<td>512GB</td>
</tr>
</tbody>
</table>

- Toshiba/SanDisk has the cheapest die and cheaper cost per Gb, this is due to the technic that is used and therefore enabling more production of dies per wafer 12-inch wafer.
- The Toshiba/SanDisk process is easier to perform compared to the Charge trap deposition.
- The Micron process of using polysilicon floating gate can be an advantage in the cost as this avoids etching out polysilicon to deposit tungsten word lines and this also reduces the etching steps.
- Micron's 96-layer process cost/Gb is still competitive compared to the 92- and 96-layer NAND memories.
Component Price - Micron

<table>
<thead>
<tr>
<th>Q3 2019</th>
<th>Q4 2019</th>
<th>Q1 2020</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Component price of NAND Flash could also vary as the NAND Flash market is highly affected by seasonal demands, shipping supply chain and production yield.

By using ASP provided by Yole for 3D NAND TLC, we estimate that Intel could realize a gross margin in the range of % between 2019 and 2020, which results in a final component price ranging from $ in 2019 to $ in 2020.
Related Reports

REVERSE COSTING ANALYSES - SYSTEM PLUS CONSULTING

MEMORY
- LPDDR4 Memory Comparison 2019
- Samsung 3D V-NAND 92 layers Memory
- Leading-edge 3D NAND Memories Comparison 2018

MARKET AND TECHNOLOGY REPORTS - YOLE DÉVELOPPEMENT

MEMORY
- DRAM & NAND Service – Memory Research
- Status of the Memory Industry 2019
Business Models Fields of Expertise

- Custom Analyses
  (>130 analyses per year)
- Reports
  (>60 reports per year)
- Costing Tools
- Trainings

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Cost Analysis
Cost Analysis Comparison
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