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Executive Summary

In automotive applications, radio-frequency (RF) complementary metal-oxide-semiconductor (CMOS) is the next technology generation for radar integrated circuits (ICs). Among its advantages, low power consumption is the main benefit. This could be attractive to other domains, like the Internet of Things. Indeed, the small form factor, along with the low power consumption, could be suitable for applications like garbage monitoring or parking regulation. Acconeer, a Swedish company, has developed and started to produce a chip that could be used in these applications, the A111. In addition to RFCMOS, the company has chosen an Antenna-in-package (AiP) technology in order to provide the smallest form factor.

This makes the A111 the most integrated radar chipset currently available on the market. It features two channels, one receiver and one transmitter, along with a controller, power management and a timing block, all on the same die. This chipset is extremely compact compared to other products on the market.

With this component Acconeer mainly targets industrial applications using pulsed coherent radar (PCR) technology. The system is designed for high-precision measurement and ultra-low power. The baseband, the RF Front-End and the antenna are delivered in a single package. The System-on-Chip for the signal processing is placed in flip-chip configuration under a printed circuit board featuring the antennas and the solder balls. By having the AiP and the PCR technology in the same device, Acconeer produces a low cost, low power, millimeter-level accuracy and high update frequency device.

This report reviews the A111, including a complete die analysis, cost analysis, and price estimate for the chips. Also included is a physical and technical comparison with Texas Instruments’ IWR6843AoP.
Package View & Dimensions

- **Package:**
- **Dimensions:**
- **Pitch:**

- **Marking:**

Package Top View
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Package Bottom View
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Package Side View
©2019 by System Plus Consulting
Package Cross-Section

Package Cross-Section Plan
©2019 by System Plus Consulting

Package Cross-Section – SEM View
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Package Opening
Package Overview

- Parts area:
  - High Frequency RFCMOS:
  - Low frequency CMOS:

A111 Schematic Diagram
Accenier
Die View & Dimensions

- Die Area:

- Nb of PGDW per 12-inch wafer:

- Pad number:
Die Overview – RF/Analog Subsystem
Die Process

- The process uses CMOS transistors
- MOS transistor gate length:
60-GHz Antenna-in-Package – External Package Comparison

- Package:
- Dimensions:
- Pitch:

Texas Instruments – IWR6843AoP – Optical View

Acconeer – A111 – Optical View
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## Front-End Cost

<table>
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<td>Foundry Gross Profit</td>
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**MMIC Front-End Price**

Acconeer outsource the manufacturing of the front-end steps **[43]**.

The **front-end cost** for the Radar IC ranges from **[44]** to **[45]**, according to yield variations.

The largest portion of the manufacturing cost is due to the **[46]**.

We take into account a gross margin of **[47]** to estimate the wafer price ranges from **[48]** to **[49]**, according to yield variations..
We estimate that Acconeer realizes a gross margin of [ ] on the component, which results in a final component price ranging from [ ].

This corresponds to the selling price for large volume to OEMs.
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- Antenna for 5G and 5G-related Applications – Patent Landscape Analysis
Contact

Headquarters
22 bd Benoni Goullin
44200 Nantes
FRANCE
+33 2 40 18 09 16
sales@systemplus.fr

Europe Sales Office
Lizzie LEVENEZ
Frankfurt am Main
GERMANY
+49 151 23 54 41 82
llevenez@systemplus.fr

America Sales Office
Steve LAFERRIERE
Phoenix, AZ
WESTERN US
T : +1 310 600 8267
laferriere@yole.fr
Chris YOUMAN
EASTERN US & CANADA
T : +1 919 607 9839
chris.youman@yole.fr

Asia Sales Office
Takashi ONOZAWA
Tokyo
JAPAN
T : +81 804 371 4887
onozawa@yole.fr
Mavis WANG
TAIWAN
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