Advanced packaging technology in the Apple Watch Series 4’s System-in-Package

Four major packaging technologies: ASE’s SiP & modified SESUB, TSMC’s inFO-ePoP, Skyworks’ Double Side BGA.

Since 2015, Apple has released five different generations of smartwatches. Each generation was built around a System-in-Package integrating all the components from the application processor to the Power Management Integrated Circuit (PMIC). In the second generation, the SiP used single side molding technology. The third generation brought Long Term Evolution (LTE) standard wireless communication through additional components soldered beneath the SiP. This year, for the fourth generation, several supplying companies have integrated their latest advanced packaging technology in order to offer the smallest and most integrated SiP since the beginning of the Apple Watch Series. In doing so each company, from foundries like TSMC to Outsourced Semiconductor Assembly and Test (OSAT) companies like ASE, has shown their High-Volume Manufacturing (HVM) capabilities.

The Series 4 smartwatch comes with two versions of the SiP. The first is a non-cellular version, with single side molding and an Inertial Measurement Unit (IMU) and a GPS Front-End Module (FEM) soldered beneath the package. The second, analyzed in this report, is the cellular version with additional Radio Frequency (RF) FEM, inside and outside the SiP, and a baseband processor included in the packaging, all in a single package smaller than 700 mm², representing 40% of the watch’s form factor.

Since the first generation, the system has used innovative packaging technology from ASE to form the SiP. It features internal shielding isolating the RF area from the other components. In this generation, Apple has chosen TSMC to provide the application processor packaging with its latest integrated Fan-Out (inFO) technology, called inFO-ePoP. Finally, Apple has used two more advanced packaging technologies to integrate a PMIC and an RF FEM in such a small form factor. The first uses embedded die technology, coupling several passives on a printed circuit board (PCB), and the IC soldered beneath. The second uses double-sided Ball Grid Array (BGA) technology to integrate a switch at the bottom of a SiP including several filters and power amplifiers.

The report will include a complete analysis of the SiP, featuring die analyses, packaging processes and cross-sections. It will also include, first, a comparison between TSMC’s inFO technology since the A9, a cost estimation of a single side RF FEM SiP and a double-side BGA, and second, a comparison with the non-cellular version of the S4 SiP.

COMPLETE TEARDOWN WITH
- Detailed photos and cross-sections
- Precise measurements
- Material analysis
- Manufacturing process flow
- Supply chain evaluation
- Manufacturing cost analysis
- Estimated sales price
ADVANCED PACKAGING TECHNOLOGY IN THE APPLE WATCH SERIES 4'S SYSTEM-IN-PACKAGE

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