Apple Watch Series 4 System-in-package

Advanced Packaging technology for SiP from TSMC, ASE, Skyworks

Packaging report by Stéphane ELISABETH

January 2019 – version 1
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Executive Summary

This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the Apple Watch Series 4 SiP.

- The smartwatch came with two versions of the SiP. The first is a non-cellular version with a single side molding and soldered beneath the package, an IMU and a GPS Front-End Module (FEM). The second, analyzed in this report, is the cellular version with additional RF FEM, inside and outside the SiP, and a baseband processor included in the packaging, all in a single package smaller than 700 mm², representing 40 % of the watch form factor.

- Since the first generation, the system uses the innovative packaging technology from ASE to form the SiP. It features internal shielding isolating the RF Area from the other components. In this generation, Apple has chosen TSMC to provide the Application processor packaging with its integrated Fan-Out (inFO) technology in the last version, called inFO-ePoP. Finally, two more advanced packaging has been considered by Apple, to integrate in such a small form factor a PMIC and a RF FEM. The first uses embedded die technology coupling several passives on a PCB and the IC soldered beneath. The second uses double-side BGA technology to integrate a Switch at the bottom of a SiP including several filters, and power amplifiers.

- The report will include a complete analysis of the SiP, featuring die analyses, packaging processes and cross-sections. It will also include, first, a comparison between the TSMC’s inFO technology since the A9, a cost estimation of a single side RF FEM SiP and a double-side BGA, and second, a comparison with the non-cellular version of the S4 SiP.
Apple Watch Series – SiP

• From the second generation of the Apple Watch, the SiP integrate monolithically all the components. For the Watch series 4, the non cellular version spread around the passive components.
Apple Watch Series 4 Cellular Teardown

Apple Watch Series 4 Opened
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Apple Watch Series 4 – Main Board
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Summary of the Physical Analysis – ASE’s SiP

SiP Assembly:
- Double Side SMD/Flip Chip assembly
- Pick & place Components on PCB substrate
- Electrical Connections and support: 10-Layers
- Special Features: Metal Coating, Shielding Walls
Summary of the Physical Analysis – TSMC’s inFO-ePoP

**inFO Assembly:**
- Fan Out Die First Face Up assembly
- Pick & place Components on Carrier Wafer
- Electrical Connections and support:

**APE Die:**
- Process:
  - CMOS 10 nm 14M
- Placement: Flip Chip on Glass Carrier
Summary of the Physical Analysis – ASE’s SESUB

**SESUB Assembly:**
- Embedded Die assembly
- Pick & place Components on PCB Substrate
- Electrical Connections and support:
- Special Features: Through Molding Via

**PMIC Die:**
- Process:
- Placement: Flip Chip on PCB Substrate

Apple Watch Series 4 – S4 PMIC Assembly
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Summary of the Physical Analysis – Skyworks’s Double Side BGA SiP

Double Side BGA SiP Assembly:
- Double Side SMD/Flip Chip assembly
- Pick & place Components on PCB Substrate
- Electrical Connections and support:

Power Amplifier Die:
- Process:
- Placement: Wire Bonded on PCB Substrate

Switch Die:
- Process:
- Placement:

RFIC Die:
- Process:
- Placement:

IPD Die:
- Process:
- Placement: Soldered on PCB Substrate
Module Opening

**Physical Analysis**
- Module Disassembly
  - Views & Dimensions
  - Cross-Section
- TSMC's inFO-ePoP
  - Views & Dimensions
  - Cross-Section
  - Die View & Dimensions
- ASE’s Double Side Molding/SESUB
  - Views & Dimensions
  - Cross-Section
  - Die View & Dimensions
- Skyworks’ FEM Double Side BGA
  - Views & Dimensions
  - Cross-Section
  - Die View & Dimensions

**Physical Comparison**

**Manufacturing Process Flow**

**Cost Analysis**

**Related Reports**

**About System Plus**

Module Cross-Section – Internal Shielding
Package Cross-Section – Through inFO Via (TiV)
Package Views & Dimensions

- Package:
- Dimensions:
- Pin Pitch:

Package Top View – Optical View
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Package Cross-Section – PCB Substrate

Physical Comparison
Manufacturing Process Flow
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Package Views & Dimensions

- Package:
- Dimensions:
- Pin Pitch:

Package Top View – Optical View
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Package Bottom View – Optical View
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Package Side View – Optical View
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Package Cross-Section – External Shielding

Physical Analysis
- Module Disassembly
  - Views & Dimensions
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- TSMC’s inFO-ePop
  - Views & Dimensions
  - Cross-Section
  - Die View & Dimensions
- ASE’s Double Side Molding/SESUB
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  - Die View & Dimensions
- Skyworks’ FEM Double Side BGA
  - Views & Dimensions
  - Cross-Section
  - Die View & Dimensions

Physical Comparison

Manufacturing Process Flow

Cost Analysis

Related Reports

About System Plus
Apple Watch S4 – Non-Cellular vs. Cellular
Global Overview – ASE’s SiP

- A12 using TSMC’s inFO-ePoP
- PMIC using ASE’s Double Side Molding
- FEM using Skyworks’s Double Side BGA

Apple Watch S4
Assembly in SiP Package
Final test
## inFO-ePoP Packaging Wafer Cost

<table>
<thead>
<tr>
<th>Package Manufacturing</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass Carrier Wafer Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield losses Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### APE Die Cost

<table>
<thead>
<tr>
<th>Dies per Reconstruct Wafer</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
</table>

### Package Manufacturing Cost Breakdown

The **Packaging cost** for the inFO ranges from [ ] according to yield variations.

The largest portion of the manufacturing cost is due to the [ ].
## inFO-ePoP Packaging Wafer & Die Cost

<table>
<thead>
<tr>
<th>Component Cost Breakdown (Medium Yield)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Cost</td>
</tr>
<tr>
<td>inFO Packaging cost</td>
</tr>
<tr>
<td>MCP Memory Price</td>
</tr>
<tr>
<td>Final Test cost</td>
</tr>
<tr>
<td>BE - Yield losses</td>
</tr>
</tbody>
</table>

### Cost Analysis Summary

- Yields Explanation & Hypotheses
  - TSMC's inFO-ePoP
  - ASE's Double Side Molding
  - Skywork's Double Side BGA
  - ASE's SIP

### Related Reports

- About System Plus

### Overhead / Introduction

### Company Profile & Supply Chain

### Physical Analysis

### Physical Comparison

### Manufacturing Process Flow

### Cost Analysis

- Cost Analysis Summary
  - Yields Explanation & Hypotheses
    - TSMC's inFO-ePoP
    - ASE's Double Side Molding
    - Skywork's Double Side BGA
    - ASE's SIP

### Component Cost

<table>
<thead>
<tr>
<th>Component</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
<td>Breakdown</td>
</tr>
</tbody>
</table>

By adding the final test cost, the **component cost** ranges from [ ] according to yield variations.

- The **die (Application processor)** represent [ ] of the component cost.
- We assume that the **Memory Component** represent [ ] of the component cost.
- The **inFO packaging** represent [ ] of the component cost.
- **Final test and yield losses** represent [ ] of the component cost.

We estimate a **gross margin** [ ] for TSMC, which result in a **component price** ranging from [ ] to [ ]. This correspond to the selling price to Apple.
Related Reports

REVERSE COSTING ANALYSES - SYSTEM PLUS CONSULTING

PACKAGING
- Samsung Exynos 9110 with ePLP: First Generation of Samsung’s Fan-Out Panel Level Packaging (FO-PLP)
- Samsung’s Galaxy S9 Plus Processor Packages: Samsung’s iPop vs. Qualcomm/Shinko MCEP
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