Samsung Exynos 9110 with ePLP: First Generation of Samsung’s Fan-Out Panel Level Packaging (FO-PLP)

The first ultra-small multi-chip High Volume Manufacturing (HVM) FO-PLP device for consumer applications found in the Samsung Galaxy Watch.

Until 2018, Samsung integrated its Application Processor Engine (APE) in standard Package-on-Package (PoP) packaging. Starting this year, with the Exynos 9810 in the Samsung Galaxy S9, Samsung has brought a new packaging technology called iPoP. And following this new packaging integration, the company has also introduced a breakthrough technology using Fan-Out Panel Level Packaging (FO-PLP) in its latest smartwatch, the Samsung Galaxy Watch. Dealing with the dimensions and footprint constraints of the watch world, Samsung has managed to bring together an APE and a Power Management Integrated Circuit (PMIC) in the same package in System-in-Package (SiP)-PoP configuration.

This complete tiny solution is integrated on the main board of the Samsung Galaxy Watch. The module includes the Exynos 9110 application processor, and Samsung’s Power management system all in a single package smaller than 80 mm². This is the second multi-chip Fan-Out device we have found on the market, but the first for a consumer product, which could be a key milestone for Fan-Out SiP technology.

The system uses advanced panel-level packaging developed by Samsung-SEMCO. It has innovative interconnections, enabling a Package-on-Package (PoP) configuration with Samsung’s in-house DRAM memory chip. The interconnections are made with an embedded structure along with the PMIC and the APE in a molded substrate on four redistribution layers (RDL).

Dedicated to smart watch application, the module has to be extremely power-efficient with a low z-height and good thermal dissipation. Thanks to the FO-PLP technology applied to this SiP, Samsung could realize the smallest form factor, lowest power and highest performance solution on the market.

The report includes a complete analysis of the SiP FO-PLP, featuring die analyses, processes and package cross-sections. It also includes a comparison with Nepe’s Distributed Chip Packaging (DCP) technology applied in the NXP SCM-i.MX6Q, TSMC’s integrated Fan-Out (iFO) technology applied to the Apple A11 and Shinko’s Molded Core embedded Packaging (MCEP) technology applied to the Qualcomm Snapdragon 845.

COMPLETE TEARDOWN WITH
• Detailed photos and cross-sections
• Precise measurements
• Material analysis
• Manufacturing process flow
• Supply chain evaluation
• Manufacturing cost analysis
• Estimated sales price
• Comparison with Nepe’s FO-WLP SiP and TSMC’s iFO technology
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