Samsung ePLP for the Exynos 9110

First multi die HVM FOPLP in a PoP configuration for consumer application

Packaging report by Stéphane ELISABETH
November 2018 – version 1
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Executive Summary

This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the Samsung Exynos 9110.

This complete tiny solution is integrated on the main board of the Samsung Galaxy Watch. The module includes the Exynos 9110 application processor, and a Samsung’s Power management system all in a single package smaller than 80 mm². This is the second multi die fan-out device than we have found in the market, but the first from such large company which could be a key milestone for Fan-Out SiP technology.

The system uses an innovative panel-level packaging developed by Samsung. It has innovative interconnections, enabling a Package-on-package (PoP) configuration with Samsung’s in-house DRAM memory Chip. A Fan-Out substrate used in a panel configuration allows memory stacking. The Fan-Out Substrate, the PMIC and the APE are embedded in a mold substrate on four redistribution layers (RDL).

Dedicated to a smart watch application, the module has to be extremely power efficient with a low z-height and a good thermal dissipation feature. Thanks to the ePLP packaging technology applied to this SiP, Samsung could realize the smaller form factor, lowest power and highest performance solution on the market.

The report will include a complete analysis of the SiP, featuring die analyses, processes and package cross-sections. It will also include a comparison with Nepes’ Redistributed Chip Packaging (RCP) technology applied in the NXP SCM-i.MX6Q, TSMC’s inFO technology applied to the Apple A11 and Shinko’s MCeP applied to the Qualcomm Snapdragon 845.
Samsung FO-PLP Packaging

Overview / Introduction
Company Profile & Supply Chain
- Samsung
- Exynos 9 Series
- Fan-Out Packaging
  - Samsung’s ePLP
- Samsung Galaxy Watch Teardown

Market Analysis
Physical Analysis
Physical Comparison
Manufacturing Process Flow
Cost Analysis
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About System Plus

Source: R. Bae, IWLP 2018

Source:
FOPLP Market Forecast

PLP market forecast, 2017-2023 (in $M)
Summary of the Physical Analysis

ePLP Assembly:

APE Die:
- Process: [ ]
- Placement: [ ]

PMIC Die:
- Process: [ ]
- Placement: [ ]

Panel Substrate

PMIC

APE

RDLs

Packaging Assembly
- O Views & Dimensions
- O RDL Deprocessing
- O Opening
- O Cross-Section
- O Process & Synthesis

Physical Analysis

Physical Comparison

Manufacturing Process Flow

Cost Analysis

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Samsung Exynos 9110 Assembly
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Package View & Dimensions

- Package:
- Dimensions:
- Pin Pitch:

Package Top View – Optical View
©2018 by System Plus Consulting

Package Bottom View – Optical View
©2018 by System Plus Consulting
• **Measured Line/Space Width in Bottom view:**
  • RDL #1:
Memory Package Opening

Package Opening View – Optical View
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Package Cross-Section – RDL

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FOPLP Process

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  - Die Cross-section

Physical Comparison

Manufacturing Process Flow

Cost Analysis

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APE Die Cross-Section – Transistors

- MOS transistor Fin pitch:
- MOS transistor Contacted gate pitch:

10 nm.
PMIC Die Views & Marking

- Die Area:

- Nb of PGDW per 4-inch wafer:

- Pad number:

- Pad Pitch:
Comparison with PoP Solutions – TSMC’s inFO

- TSMC’s inFO min. Line/Space width:
- Samsung’s ePLP SiP min. Line/Space width:

Samsung’s ePLP Package
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TSMC’s inFO
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Package Comparison – PoP Technology

**Standard PoP**

**MCeP**

**inFO**

**ePLP**

---

**Board Cross-Section – Optical View**

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Package Comparison – FO-SiP

- **PCB Frame Area:**
- **PCB Frame package Fill Factor:**

- **PCB Frame Area:**
- **PCB Frame package Fill Factor:**
Packaging Process Flow

The package is manufactured and assembled by Samsung in South Korea.

- **FOPLP Process:**
  - Package Type:
  - Carrier:
  - Process type:

- **Test:**
  - Test type:
FOPLP – Process Flow (2/5)

- Panel Substrate
- Panel Substrate
- Dummy Substrate
- Dummy Substrate
- Dummy Substrate
### ePLP Packaging process

#### Cost Analysis
- Cost Analysis Summary
- Yields Explanation & Hypotheses
- APE & PMIC Wafer FE Cost
- APE & PMIC Prep. Wafer Cost
- APE & PMIC Die Cost
- ePLP Packaging Cost
- Component Cost

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#### Package Manufacturing Cost Breakdown (Medium Yield)

The **Packaging cost** for the ePLP ranges from [ ] according to yield variations.

The largest portion of the manufacturing cost is due to the [ ]
Related Reports

**REVERSE COSTING ANALYSES - SYSTEM PLUS CONSULTING**

PACKAGING
- NXP SCM-IMX6Q RCP Fan-Out SiP
- Apple A11 with second generation of TSMC’s inFO
- Samsung Galaxy S9’s Application Processor: Exynos 9810 vs. Qualcomm Snapdragon 845
- Intel’s Embedded Multi-Die Interconnect Bridge (EMIB)

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