Texas Instruments AWR1642

All-in-one 79 GHz Radar Chipset

RF report by Stéphane ELISABETH
April 2018 – version 1
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Executive Summary

• The Texas Instruments’ portfolio contains three different chip configurations from low power and highly integrated device to high performance radar working in the 79 GHz band. The AWR1642 is the most integrated radar chip that we can find now on the market. It features six channels (four receivers and two transmitters) along with an MCU and a DSP all on the same chip.

• Working in the 79 GHz, Texas Instrument target the replacing market on 24 GHz short range application that will decrease in 2020 with the coming European restriction law.

• Also having the control unit and the signal processing chip on the same die, it allows to reduce drastically the PCB footprint of the solution with almost 60% of space reduction compared to a separate solution.

• This report analyses the AWR1642 including a complete analysis of the die along with a cost analysis and a price estimate for the chips. It also includes a physical and technical comparison with a Delphi’s SRR chipset solution and the Texas Instrument AWR1243 featuring four receivers and three transmitters without the MCU and the DSP targeting Long Range Radar detection and Radar imaging.
Market Analysis

Chip market forecast ($M)

Chip market forecast by technology split ($M)

- RF CMOS
- SiGe Bi-CMOS
- GaAs
Package View & Dimensions

- Package:
- Dimensions:
- Pitch:

Package Top View
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Package Bottom View
©2018 by System Plus Consulting

Package Side View
©2018 by System Plus Consulting
Package Cross-Section

- Copper Line Thickness:
  - Line #1:
  - Line #2:
  - Line #3:
  - Line #4:

- Dielectrics Layers Thickness:
  - Solder Mask:
    - Line #1:
    - Prepreg:
    - Line #2:
    - Solder Mask:

- Micro-Via Dimension:
  - Diameter:
  - Depth:

- Measured Line/Space Width in Cross-Section:
  - 
Package Opening
Die Overview – RF/Analog Subsystem

Die Overview

Variable Gain Amplifier

Analog-to-Digital Converter (ADC)

Bandpass filter

Mixer

Low noise Amplifier

Receiver Schematic

Texas Instruments patent US 565835962
Die Process – CMOS Transistor

- The process uses CMOS transistors:
  - MOS transistor gate length:
- The gate length measurement lets us think that the technology node is
• The process uses metal layers.
# Integrated Solution vs. Separated solution (SRR Solution)

<table>
<thead>
<tr>
<th>Product</th>
<th>Packaging Area</th>
<th>Packaging Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receiver AFE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency Synthesizer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receiver</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transmitter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Delphi Solutions

- MCU & DSP included

## Texas instruments Solution

<table>
<thead>
<tr>
<th>Product</th>
<th>Packaging Area</th>
<th>Packaging Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>AWR1642</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Reduction in Area

* Assuming 1 mm spacing between packaging on PCB faces without any EMI consideration.

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Front-End Cost

<table>
<thead>
<tr>
<th>Front-End</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Raw wafer Cost (Si)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield losses Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Texas Instruments outsource the manufacturing of the front-end steps.

The **front-end cost** for the Radar IC ranges from $\_\_\_\_\_\_\_\_\_\_ to $\_\_\_\_\_\_\_\_\_\_\_ according to yield variations.

The largest portion of the manufacturing cost is due to the **wafer & die cost**.

We take into account a gross margin of $\_\_\_\_\_\_\_\_\_\_\_ to estimate the wafer price ranges from $\_\_\_\_\_\_\_\_\_\_\_\_\_\_ to $\_\_\_\_\_\_\_\_\_\_\_\_\_\_ according to yield variations.
Component Cost Breakdown According to Yield Variation

- Low Yield
- Medium Yield
- High Yield

- Die cost
- Packaging cost
- Final test & Calibration cost
- Yield losses cost

Summary of the Cost Analysis
Yields Hypothesis
Wafer & Die Cost
Component Cost

Selling Price Analysis
Feedbacks
About System Plus
### 79 GHz RFCMOS Radar Chipset Estimated Selling Price

<table>
<thead>
<tr>
<th>Component cost</th>
<th>Cost</th>
<th>Breakdown</th>
<th>Cost</th>
<th>Breakdown</th>
<th>Cost</th>
<th>Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td>Texas Instruments Gross Profit</td>
<td>Low Yield</td>
<td>Medium Yield</td>
<td>High Yield</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

We estimate that Texas Instruments realizes a gross margin on the Radar Chipset, which results in a final component price ranging from

This corresponds to the selling price for large volume to OEMs.
Related Reports

**REVERSE COSTING ANALYSES - SYSTEM PLUS CONSULTING**

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- Delphi Rear and Side Detection System
- Continental SRR3 – B 24GHz Blind - Spot Radar

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