Texas Instruments LMG5200
80V GaN Power Stage
Power Semiconductor report by Elena Barbarini

February 2018 – sample
SUMMARY

Overview / Introduction
- Executive Summary
- Reverse Costing Methodology

Company Profile
- Texas Instruments

Physical Analysis
- Synthesis of the Physical Analysis
- Package analysis
  - Package opening
  - Package Cross-Section
- FET Die
  - FET Die View & Dimensions
  - FET Die Process
  - FET Die Cross-Section
  - FET Die Process Characteristic
- IC Die
  - IC Die View & Dimensions
  - IC Die Process
  - IC Die Cross-Section
  - IC Die Process Characteristic

Power Stage Manufacturing Process
- FET Die Front-End Process
- FET Die Fabrication Unit
- IC Die Front-End Process
- IC Die Fabrication Unit
- Final Test & Packaging Fabrication unit

Cost Analysis
- Synthesis of the cost analysis
- Yields Explanation & Hypotheses
- FET die
  - FET Front-End Cost
  - FET Die Probe Test, Thinning & Dicing
  - FET Wafer Cost
  - FET Die Cost
- IC die
  - IC Front-End Cost
  - IC Die Probe Test, Thinning & Dicing
  - IC Wafer Cost
  - IC Die Cost
- Complete Power Stage
  - Packaging Cost
  - Final Test Cost
  - Component Cost

Price Analysis
- Estimation of selling price

Comparison
- Comparison between Panasonic, Transphorm and GaN Systems HEMT

Feedback

System Plus services
Executive Summary

To minimize the parasites linked to high frequency operations and to propose a driver integrated solution, Texas Instruments has introduced the first 80V Half bridge GaN FET power stage device in advanced QFM package.

In this report System Plus Consulting unveils TI’s technical choices; from the device design up to the packaging. It is the first time that we can find a Half bridge design GaN FET with its driver, all assembled in an advanced multichip packaging.

The new LMG3410 from TI features a GaN FET with a breakdown voltage of 80V for a current of 10A (25°C). The transistor is driven by a National Semiconductors silicon IC Gate driver with 1 µm technology node.

The epitaxy structure is composed of different GaN and AlGaN layers and multiple heterojunction structure of AlGaN between GaN and the AlN layer. A complex buffer and template layers’ structure is used to reduce the stress and the dislocation.

Based on a complete teardown analysis, the report also provides an estimation of the production cost of the IC Gate driver, the FET and the package.

Moreover, the report proposes a comparison with the GaN Systems, Transphorm and Panasonic packaging and epitaxy. This comparison highlights the differences in design and manufacturing process and their impact on device size and production cost.
Synthesis of the Physical Analysis

Package QFM:
- Advanced multichip packaging
- Dimensions: 6mm x 8mm x 2mm
- Number of Pins: x pin

FET:
- Dimension: xxxmm x xxxmm = xxx mm²
- Electrical Connection: xxx
- Placement in the package: xxx on copper lead frame.

IC:
- Dimension: xxx mm² (xxxmm x xxxmm)
- Electrical Connection: xxx
- Placement in the package: xxx.
Package Opening – From back side

- Micro vias: xxx
Device design

Overview / Introduction
Company Profile & Supply Chain
Physical Analysis
  - Synthesis
  - Package
  - GaN FET
  - IC
Manufacturing Process Flow
Cost Analysis
Selling Price Analysis
Comparison
Feedback
About System Plus

Package Opening

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>7</td>
<td>Analog ground. Ground of power devices</td>
</tr>
<tr>
<td>HS</td>
<td>2</td>
<td>High-side gate driver high-side rail</td>
</tr>
<tr>
<td>H1</td>
<td>4</td>
<td>High-side gate driver high-side input</td>
</tr>
<tr>
<td>HS</td>
<td>3</td>
<td>High-side GaN FET source connection</td>
</tr>
<tr>
<td>L</td>
<td>5</td>
<td>Low-side drain control in/out</td>
</tr>
<tr>
<td>PDN</td>
<td>9</td>
<td>Power pin. Low-side GaN FET driver. Electrically shorted to GND pin</td>
</tr>
<tr>
<td>SW</td>
<td>8</td>
<td>Switching node. Electrically shorted to HS pin. Ensure live clearance at this point on PCB</td>
</tr>
<tr>
<td>VCC</td>
<td>6</td>
<td>Positive gate drive input</td>
</tr>
<tr>
<td>VIN</td>
<td>1</td>
<td>Input voltage pin. Electrically connected to high-side GaN FET drain.</td>
</tr>
</tbody>
</table>
Package Cross-Section
Package Cross-Section – Laminate Substrate

- The package laminate is a xxx layers PCB.
  - PCB thickness: \(xxx \, \mu m\)
  - Copper layers thickness: \(xxx \, \mu m\)
  - Microvia diameter: \(xxxx \, \mu m\)
FET die Dimensions

- Die dimensions: xxx mm² (xxxmm x xxxmm)
- There is no marking on the die
Die process

Transistor process after delayering – SEM View
Die cross section

- Substrate thickness: xxx µm
Die cross section

- Overview / Introduction
- Company Profile & Supply Chain
- Physical Analysis
  - Synthesis
  - Package
  - GaN FET
  - IC
- Manufacturing Process Flow
- Cost Analysis
- Selling Price Analysis
- Comparison
- Feedback
- About System Plus
Die cross section – Gate & source
Die cross section - Gate

Die cross section – SEM View
EDX epitaxy

Company Profile & Supply Chain
- Physical Analysis
  - Synthesis
  - Package
    - GaN FET
  - IC

Manufacturing Process Flow
- Cost Analysis
- Selling Price Analysis
- Comparison
- Feedback
- About System Plus
IC die Dimensions

- Die dimensions: \( xxx \text{ mm}^2 \) (\( xxx \text{ mm} \times xxx \text{ mm} \))
- Connected pads: 12
Die Process

Overview / Introduction

Company Profile & Supply Chain

Physical Analysis
  - Synthesis
  - Package
  - GaN FET
  - IC

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

Comparison

Feedback

About System Plus

LDMOS transistors are present on the circuit.
Die cross section

- Substrate thickness: xxx µm
Die cross section

The process uses 3 metal layers in Aluminum with planarization. There are tungsten plugs between the metal layers.
GaN Transistor - Process Flow (2/4)

- Implantation in the AlGaN layer
- Implantation in the gate GaN layer

- Pattern and GaN etching

- TiN deposition
- Pattern Gate Metal

Drawing not to Scale
GaN Transistor - Solder Bumps

- Probe test
- Polyimide deposition and pattern
- UBM

- Solder bumps electroplating
- Solder reflow

- Dicing
In our simulation, we assume a development and a production ramp up without important technical problems.
Wafer Front-End Cost

The front-end cost ranges from $xxx to $xxx according to yield variations.

The main part of the wafer cost is due to the xxxx with xxx%. The epitaxy steps represent a large part of consumable and equipment cost (see details in the following pages).
The FET Component cost ranges from $xxx to $xxx according to yield variations.

The Front-end manufacturing represents xxx% of the component cost (medium yield estimation).

Probe test, dicing and scrap account for xxx% of the component cost.
The die cost is estimated between $xxx and $xxx according to the yield. Silicon cost accounts for xxx% of the cost. The probe test, backgrinding and dicing represent xxx% of the cost. The scrap cost (xxx%) is the total of all the losses during the back-end process.
## Packaging Cost

### Cost Breakdown

<table>
<thead>
<tr>
<th>Package Manufacturing Cost</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unpacking PCB + dies</td>
<td>$0.0000</td>
<td>$0.0000</td>
<td>$0.0000</td>
</tr>
<tr>
<td>Cleaning PCB</td>
<td>$0.0600</td>
<td>$0.0600</td>
<td>$0.0600</td>
</tr>
<tr>
<td>Dispense</td>
<td>$0.1400</td>
<td>$0.1400</td>
<td>$0.1400</td>
</tr>
<tr>
<td>Flip chip FET</td>
<td>$0.0100</td>
<td>$0.0100</td>
<td>$0.0100</td>
</tr>
<tr>
<td>Flip chip ASIC</td>
<td>$0.0100</td>
<td>$0.0100</td>
<td>$0.0100</td>
</tr>
<tr>
<td>Placing Capa</td>
<td>$0.0000</td>
<td>$0.0000</td>
<td>$0.0000</td>
</tr>
<tr>
<td>Reflow of die on PCB</td>
<td>$0.0500</td>
<td>$0.0500</td>
<td>$0.0500</td>
</tr>
<tr>
<td>Void test (X-Ray inspection)</td>
<td>$0.0200</td>
<td>$0.0200</td>
<td>$0.0200</td>
</tr>
<tr>
<td>Underfill</td>
<td>$0.2000</td>
<td>$0.2000</td>
<td>$0.2000</td>
</tr>
<tr>
<td>Curing</td>
<td>$0.0900</td>
<td>$0.0900</td>
<td>$0.0900</td>
</tr>
<tr>
<td>DBC+die Cleaning + rinsing + drying</td>
<td>$0.0800</td>
<td>$0.0800</td>
<td>$0.0800</td>
</tr>
<tr>
<td>Encapsulation molding</td>
<td>$0.0200</td>
<td>$0.0200</td>
<td>$0.0200</td>
</tr>
<tr>
<td>Post-mold Curing</td>
<td>$0.0100</td>
<td>$0.0100</td>
<td>$0.0100</td>
</tr>
<tr>
<td>Yield losses Cost</td>
<td>$0.0946</td>
<td>$0.0774</td>
<td>$0.0617</td>
</tr>
</tbody>
</table>

### Selling Price Analysis

- **FET Die Cost**: $1.162, $1.060, $0.966
- **ASIC Die Cost**: $0.0755, $0.0732, $0.0710
- **PCB Cost**: $0.6800, $0.6800, $0.6800

### Comparison

<table>
<thead>
<tr>
<th>Package Manufacturing Cost</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unpacking PCB + dies</td>
<td>$0.0000</td>
<td>$0.0000</td>
<td>$0.0000</td>
</tr>
<tr>
<td>Cleaning PCB</td>
<td>$0.0600</td>
<td>$0.0600</td>
<td>$0.0600</td>
</tr>
<tr>
<td>Dispense</td>
<td>$0.1400</td>
<td>$0.1400</td>
<td>$0.1400</td>
</tr>
<tr>
<td>Flip chip FET</td>
<td>$0.0100</td>
<td>$0.0100</td>
<td>$0.0100</td>
</tr>
<tr>
<td>Flip chip ASIC</td>
<td>$0.0100</td>
<td>$0.0100</td>
<td>$0.0100</td>
</tr>
<tr>
<td>Placing Capa</td>
<td>$0.0000</td>
<td>$0.0000</td>
<td>$0.0000</td>
</tr>
<tr>
<td>Reflow of die on PCB</td>
<td>$0.0500</td>
<td>$0.0500</td>
<td>$0.0500</td>
</tr>
<tr>
<td>Void test (X-Ray inspection)</td>
<td>$0.0200</td>
<td>$0.0200</td>
<td>$0.0200</td>
</tr>
<tr>
<td>Underfill</td>
<td>$0.2000</td>
<td>$0.2000</td>
<td>$0.2000</td>
</tr>
<tr>
<td>Curing</td>
<td>$0.0900</td>
<td>$0.0900</td>
<td>$0.0900</td>
</tr>
<tr>
<td>DBC+die Cleaning + rinsing + drying</td>
<td>$0.0800</td>
<td>$0.0800</td>
<td>$0.0800</td>
</tr>
<tr>
<td>Encapsulation molding</td>
<td>$0.0200</td>
<td>$0.0200</td>
<td>$0.0200</td>
</tr>
<tr>
<td>Post-mold Curing</td>
<td>$0.0100</td>
<td>$0.0100</td>
<td>$0.0100</td>
</tr>
<tr>
<td>Yield losses Cost</td>
<td>$0.0946</td>
<td>$0.0774</td>
<td>$0.0617</td>
</tr>
</tbody>
</table>

### Package Manufacturing Cost

- **FET Die Cost**: $1.162, $1.060, $0.966
- **ASIC Die Cost**: $0.0755, $0.0732, $0.0710
- **PCB Cost**: $0.6800, $0.6800, $0.6800
The component cost ranges from $xxx to $xxx according to yield variations.

The FET die manufacturing represents xxx% of the component cost.

The IC die manufacturing represents xxx% of the component cost.

The packaging represents xxx% of the component cost.

Final test and yield losses account for xxx% of the component cost.
The component manufacturing cost ranges from $\text{xxx}$ to $\text{xxxx}$ according to yield variations.

The component selling price ranges from $\text{xx}$ to $\text{xxxx}$ according to yield variations.
Comparison between Transphorm, GaN Systems, Panasonic and TI GaN FET package

<table>
<thead>
<tr>
<th>FET</th>
<th>Packaging</th>
<th>Size</th>
<th>Pakage Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGA26E19BA</td>
<td>DFN 8</td>
<td>8x8x1.25</td>
<td>$xx</td>
</tr>
<tr>
<td>GS66504B</td>
<td>GaNpx embedded</td>
<td>8.7x10x0.47</td>
<td>$xx</td>
</tr>
<tr>
<td>TPH3206PS</td>
<td>TO220D cascode</td>
<td>14x10x4.5</td>
<td>$xx</td>
</tr>
<tr>
<td>LMG5200</td>
<td>QFM</td>
<td>8x6x0.9</td>
<td>$xx</td>
</tr>
</tbody>
</table>

The packaging has an high impact on the final cost and performances of the devices.

The device of TI, even if it has an integrated driver, the cost competitive.
Related Reports

**REVERSE COSTING ANALYSES - SYSTEM PLUS CONSULTING**

**Power Semiconductors & Compound**
- Panasonic PGA26C09DV 600V GaN HEMT
- Transphorm TPH3002PS 600V GaN on Silicon HEMT
- GaN Systems – 650V GaN on Silicon HEMT AT&S ECP® Embedded Power Die Package

**MARKET AND TECHNOLOGY REPORTS - YOLE DÉVELOPPEMENT**

**POWER ELECTRONICS**
- Gate Driver Market and Technology Trends 2017

**PATENT ANALYSIS - KNOWMADE**

**POWER ELECTRONICS**
- GaN Devices for Power Electronics Patent Investigation
COMPANY SERVICES
Business Models Fields of Expertise

- Custom Analyses
  (>130 analyses per year)
- Reports
  (>40 reports per year)
- Costing Tools
- Trainings

System: Power, Display, LED, IC & RF, MEMS & Sensor, PCB, Imaging, Packaging, System

About System Plus
- Company services
- Related reports
- Contact
- Legal

Company Profile & Supply Chain
Physical Analysis
Manufacturing Process Flow
Cost Analysis
Selling Price Analysis
Comparison
Feedback

©2018 by System Plus Consulting | TI LMG5200
Please process my order for “Texas Instruments’ LMG5200 80V GaN FET Power Stage” Report

Ref.: SP18363

- Full Reverse Costing report: EUR 3,490*
- Annual Subscription (including this report as the first of the year):
  - 3 reports EUR 8,400*
  - 5 reports EUR 12,500*
  - 7 reports EUR 16,000*
  - 10 reports EUR 21,000*
  - 15 reports EUR 27,500*

*For price in dollars please use the day’s exchange rate  
*All reports are delivered electronically in pdf format  
*Our prices are subject to change. Please check our new releases and price changes on www.systemplus.fr. The present document is valid 6 months after its publishing date: February 2018

SHIP TO
Name (Mr/Ms/Dr/Pr):

Job Title:

Company:

Address:

City: State:

Postcode/Zip:

Country:

vat ID Number for EU members:

Tel:

Email:

Date:

Signature:

BILLING CONTACT
First Name: 
Last Name: 
Email:
Phone:

PAYMENT
DELIVERY on receipt of payment:

By credit card:
Number: |__|__|__|__|  |__|__|__|__|  |__|__|__|__|  |__|__|__|__|
Expiration date: |__|__|/|__|__|  Card Verification Value: |__|__|__|

By bank transfer:
HSBC - CAE- Le Terminal -2 rue du Charron - 44800 St Herblain France
BIC code: CCFRFRPP

In EUR
Bank code: 30056 - Branch code: 00955 - Account: 09550003234
IBAN: FR76 3005 6009 5509 5500 0323 439

In USD
Bank code: 30056 - Branch code: 00955 - Account: 09550003247
IBAN: FR76 3005 6009 5509 5500 0324 797

Return order by:
FAX: +33 2 53 55 10 59
MAIL: SYSTEM PLUS CONSULTING
21 rue La Noué Bras de Fer
44200 Nantes – France

Contact:
EMAIL: sales@systemplus.fr
TEL: +33 2 40 18 09 16

ABOUT SYSTEM PLUS CONSULTING
System Plus Consulting is specialized in the cost analysis of electronics from semiconductor devices to electronic systems. A complete range of services and costing tools to provide in-depth production cost studies and to estimate the objective selling price of a product is available.

Our services:
TECHNOLOGY ANALYSIS - COSTING SERVICES - COSTING TOOLS - TRAININGS

www.systemplus.fr - sales@systemplus.fr
1. INTRODUCTION
The present terms and conditions apply to the offers, sales and deliveries of services managed by System Plus Consulting except in the case of a particular written agreement. Buyer must note that placing an order means an agreement without any restriction with these terms and conditions.

2. PRICES
Prices of the purchased services are those which are in force on the date the order is placed. Prices are in Euros and worked out without taxes. Consequently, the taxes and possible added costs agreed when the order is placed will be charged on these initial prices. System Plus Consulting may change its prices whenever the company thinks it necessary. However, the company commits itself in invoicing at the prices in force on the date the order is placed.

3. REBATES and DISCOUNTS
The quoted prices already include the rebates and discounts that System Plus Consulting could have granted according to the number of orders placed by the Buyer, or other specific conditions. No discount is granted in case of early payment.

4. TERMS OF PAYMENT
System Plus Consulting delivered services are to be paid within 30 days end of month by bank transfer except in the case of a particular written agreement. If the payment does not reach System Plus Consulting on the deadline, the Buyer has to pay System Plus Consulting a penalty for late payment the amount of which is three times the legal interest rate. The legal interest rate is the current one on the delivery date. This penalty is worked out on the unpaid invoice amount, starting from the invoice deadline. This penalty is sent without previous notice. When payment terms are over 30 days end of month, the Buyer has to pay a deposit which amount is 10% of the total invoice amount when placing his order.

5. OWNERSHIP
System Plus Consulting remains sole owner of the delivered services until total payment of the invoice.

6. DELIVERIES
The delivery schedule on the purchase order is given for information only and cannot be strictly guaranteed. Consequently any reasonable delay in the delivery of services will not allow the buyer to claim for damages or to cancel the order.

7. ENTRUSTED GOODS SHIPMENT
The transport costs and risks are fully born by the Buyer. Should the customer wish to ensure the goods against lost or damage on the base of their real value, he must imperatively point it out to System Plus Consulting when the shipment takes place. Without any specific requirement, insurance terms for the return of goods will be the carrier current ones (reimbursment based on good weight instead of the real value).

8. FORCE MAJEURE
System Plus Consulting responsibility will not be involved in non execution or late delivery of one of its duties described in the current terms and conditions if these are the result of a force majeure case. Therefore, the force majeure includes all external event unpredictable and irresistible as defined by the article 1148 of the French Code Civil?

9. CONFIDENTIALITY
As a rule, all information handed by customers to system Plus Consulting are considered as strictly confidential. A non-disclosure agreement can be signed on demand.

10. RESPONSABILITY LIMITATION
The Buyer is responsible for the use and interpretations he makes of the reports delivered by System Plus Consulting. Consequently, System Plus Consulting responsibility can in no case be called into question for any direct or indirect damage, financial or otherwise, that may result from the use of the results of our analysis or results obtained using one of our costing tools.

11. APPLICABLE LAW
Any dispute that may arise about the interpretation or execution of the current terms and conditions shall be resolved applying the French law. It the dispute cannot be settled out-of-court, the competent Court will be the Tribunal de Commerce de Nantes.