Comparative Report
Silicon Capacitors
Passive Component report by Elena Barbarini & Pierre-Vincent Dugue
September 2017 – version 1
# Table of contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Overview / Introduction</strong></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>- Executive Summary</td>
</tr>
<tr>
<td></td>
<td>- Reverse Costing Methodology</td>
</tr>
<tr>
<td><strong>Company Profile</strong></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>- IPDiA Profile &amp; products</td>
</tr>
<tr>
<td></td>
<td>- Vishay Profile &amp; products</td>
</tr>
<tr>
<td></td>
<td>- Skyworks Profile &amp; products</td>
</tr>
<tr>
<td></td>
<td>- TSMC Profile &amp; products</td>
</tr>
<tr>
<td><strong>Physical Analysis</strong></td>
<td>17</td>
</tr>
<tr>
<td></td>
<td>- Synthesis</td>
</tr>
</tbody>
</table>
| | | - **IPDiA**
| | | | ✓ 935-121-427-710
| | | | ✓ 935-121-424-410
| | | | ✓ 935-121-425-610
| | | | ✓ 935-125-425-710
| | | - **Vishay**
| | | | ✓ RFCS04021500CBTT1
| | | | ✓ RFCS04024000DBTT1
| | | - **Skyworks**
| | | | ✓ SC00380912
| | | - **TSMC**
| | | | ✓ GS25 (in iPhone 7 plus) |
| **Physical comparison** | 88 |
| | - Design Comparison |
| | - Height Comparison |
| | - Material Comparison |
| | - Capacitance Analysis |
| **Manufacturing Process Flow** | 94 |
| | - Synthesis |
| | - Wafer fabrication unit |
| | - Capacitor Process Flow |
| **Cost Analysis** | 109 |
| | - Synthesis |
| | - IPDiA Cost Analysis |
| | - Vishay Cost Analysis |
| | - Skyworks Cost Analysis |
| | - TSMC Cost Analysis |
| **Selling Price** | 158 |
| | - Definition of Prices |
| | - Cost & Price |
| **Comparisons** | 171 |
| **Company services** | 173 |
Executive Summary

• This comparative report has been conducted to provide insight on technology data, manufacturing cost and selling price of different Silicon Capacitors.

• Those capacitors are designed and manufactured by the companies IPDiA, Vishay, Skyworks and TSMC.

• All of the capacitors are manufactured on a silicon substrate to increase the level of integration in complex electronic circuits.

• In this report it is present a comparison of each structures.

• Thanks to the different technologies shown on this report, Silicon capacitors are able to compete with MLCCs capacitors.
Analyzed Capacitors

- The list below regroup all the general data on the capacitors studied in this report.
- This report will include a complete study of:
  - 4 IPDiA capacitors which use a Deep trench and a Trench technology
  - 2 Vishay capacitors which use a MNOS technology
  - 1 Skyworks capacitor which uses a MIS technology
  - 1 TSMC capacitor

- A detailed study of a relation between the capacitance and the structure of those capacitors will be detailed in the Physical Comparison part.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Capacitor</th>
<th>Packaging</th>
<th>Size</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPDiA</td>
<td>935121427710-T1N</td>
<td>1206</td>
<td>6.8 mm2</td>
<td>Deep Trench Capacitor</td>
</tr>
<tr>
<td>IPDiA</td>
<td>935121424410-T3N</td>
<td>0603</td>
<td>2.25 mm2</td>
<td>Deep Trench Capacitor</td>
</tr>
<tr>
<td>IPDiA</td>
<td>935121425610-T3N</td>
<td>0402</td>
<td>0.97 mm2</td>
<td>Deep Trench Capacitor</td>
</tr>
<tr>
<td>IPDiA</td>
<td>935125425710-T1A</td>
<td>1208</td>
<td>6 mm2</td>
<td>Deep Trench Capacitor</td>
</tr>
<tr>
<td>Vishay</td>
<td>RFCS04021500CBTT1</td>
<td>0402</td>
<td>0.57 mm2</td>
<td>MNOS Capacitor</td>
</tr>
<tr>
<td>Vishay</td>
<td>RFCS04024000DBTT1</td>
<td>0402</td>
<td>0.57 mm2</td>
<td>MNOS Capacitor</td>
</tr>
<tr>
<td>Skyworks</td>
<td>SC00830912</td>
<td>0101</td>
<td>0.09 mm2</td>
<td>MIS Capacitor</td>
</tr>
<tr>
<td>TSMC</td>
<td>GS25</td>
<td></td>
<td>0.44 mm2</td>
<td>Deep Trench Capacitor</td>
</tr>
</tbody>
</table>
Synthesis of the Physical Analysis

IPDiA's Packages SMT:
- 1206 Dimensions: 3.6 mm x 1.9 mm
- 0402 Dimensions: 1.3 mm x 0.8 mm
- 0603 Dimensions: 1.9 mm x 1.2 mm
- 1208 Dimensions: 3 mm x 2 mm

- Number of Pads: 2-pad

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

About System Plus
Package Delaying (IPDiA)

### Physical Analysis
- **Synthesis**
  - IPDiA
    - 935121427710
    - 935121424410
    - 935121425610
    - 93512542S710
- **Vishay**
  - Die Vishay Capa #1
  - Die Vishay Capa #2
- **Skyworks**
  - Die Skyworks Capa #1
- **TSMC**
  - Die TSMC Capa #
- **Physical Comparison**

### Manufacturing Process Flow
1. Package Delayering (IPDiA)
2. Package 0402 - 935121424410-T3N
3. Package 1206 - 935121427710-T1N
4. Package 1208 - 93512542S710-T1A
5. Package 0603 - 9351212527710-T3N

### IPDiA Capacitors (Reference)

<table>
<thead>
<tr>
<th>Capacitors</th>
<th>Capacitance</th>
<th>Tolerance</th>
<th>Operating Temperature</th>
<th>Packaging</th>
<th>Breakdown Voltage</th>
<th>Max ESL</th>
<th>Max ESR</th>
</tr>
</thead>
<tbody>
<tr>
<td>935121427710-T1N</td>
<td>1μF</td>
<td>±15%</td>
<td>-55°C to +150°C</td>
<td>1206</td>
<td>11 VDC</td>
<td>1500mΩ</td>
<td>500mΩ</td>
</tr>
<tr>
<td>935121424410-T3N</td>
<td>1nF</td>
<td>±15%</td>
<td>-55°C to +150°C</td>
<td>0402</td>
<td>11 VDC, 30VDC</td>
<td>105mΩ</td>
<td>400mΩ</td>
</tr>
<tr>
<td>935121425610-T3N</td>
<td>100nF</td>
<td>±15%</td>
<td>-55°C to +150°C</td>
<td>0603</td>
<td>11 VDC</td>
<td>250pH</td>
<td>400mΩ</td>
</tr>
<tr>
<td>93512542S710-T1A</td>
<td>1μF</td>
<td>±15%</td>
<td>-55°C to +250°C</td>
<td>1208</td>
<td>11 VDC</td>
<td>100pH</td>
<td>100mΩ</td>
</tr>
</tbody>
</table>
Datasheet

Overview / Introduction

Company Profile & Supply Chain

Physical Analysis
- Synthesis
  - IPDIA
  - Die Vishay Capa #1
  - Die Vishay Capa #2
- Skyworks
  - Die Skyworks Capa #1
- TSMC
  - Die TSMC Capa #
- Physical Comparison

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

About System Plus

Electrical specification

<table>
<thead>
<tr>
<th>Capacitance value</th>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 nF</td>
<td>Capacitance range</td>
<td>10 nF to 1 mF</td>
</tr>
<tr>
<td></td>
<td>Capacitance tolerances</td>
<td>±1%</td>
</tr>
<tr>
<td></td>
<td>Temperature coefficient</td>
<td>±4%</td>
</tr>
<tr>
<td></td>
<td>Insulation resistance</td>
<td>15GΩ at 85°C</td>
</tr>
<tr>
<td></td>
<td>Reliability</td>
<td>2E12 bits / billion hours</td>
</tr>
<tr>
<td></td>
<td>Capacitor height</td>
<td>Max 0.2mm</td>
</tr>
</tbody>
</table>

Fig. 1 Capacitance change versus temperature variation compared with alternative dielectrics
Fig. 2 Capacitance change versus voltage variation compared with alternative dielectrics
Fig. 3 ESL versus capacitance value compared with alternative dielectrics

Part Number

935.121

i.e.: 1 µF/1206 case (LPSC type) → 935.121.427.710
Top Delayering IPDiA 935121427710-T1N (1206)

Dimensions of the device: xxx mm²

Dimensions of the trenches area: xxx mm²
Package characteristics

The die marking includes:

C1206 710 2
(size = passive 1206)
7 => 0.1µF x10 = 1µF value of the capacitor
Die Cross Section IPDiA 935121427710-T1N (1206)

Location of the section

Capacitor height measurement: xxxμm

Package 1206 cross section – SEM view
Die Cross Section IPDiA 935121427710-T1N (1206)

Overview / Introduction

Company Profile & Supply Chain

Physical Analysis
- Synthesis
- IPDiA
  - 935121427710
  - 935121424410
  - 935121425610
  - 935125425710
- Vishay
  - Die Vishay Capa #1
  - Die Vishay Capa #2
- Skyworks
  - Die Skyworks Capa #1
- TSMC
  - Die TSMC Capa #
- Physical Comparison

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

About System Plus

1206 cross section – SEM view
Top Delaying IPDiA 935121425610-T3N (0603)
Die Cross Section IPDiA 935121425610-T3N (0603)
Top Delayering Vishay RFCS04021500CBTT1

Dimensions of the device: xxx mm²

Dimensions of the active area: xxx mm²
Cross-Section Vishay RFCS04021500CBTT1
Package characteristics

- The package is LSC (Land-Side Capacitor)
  There is no markings on the capacitor
- The LSC is a high density deep trench capacitor on silicon substrate developed by TSMC using trench capacitor to increase the capacitive area without changing the footprint of the component
Die marking

The die marking includes:

tSmC
GS25
Top Delaying TSMC

Overview / Introduction

Company Profile & Supply Chain

Physical Analysis
- Synthesis
- IPDIA
  - 935121427710
  - 935121424410
  - 935121425610
  - 935125425710
- Vishay
  - Die Vishay Capa #1
  - Die Vishay Capa #2
- Skyworks
  - Die Skyworks Capa #1
- TSMC
  - Die TSMC Capa #
- Physical Comparison

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

About System Plus
Capacitance Analysis

- For the trench capacitors, 3 characteristics can change the capacitance:
  - Trenches Depth
  - Active area (area with trenches)
  - Layers of Polysilicon

- The table in the bottom reveals that the deeper the trenches, the bigger the capacitance. It can be explain because it increases the area of the electrodes coverage and therefore, the capacitance.

- The active area is one of the characteristic which plays on the capacitance parameter (see the table below).

- The layers of polysilicon: the two pictures shows how the connection is realized in the trench structure. IPDiA use the double polysilicon layer to increase the capacitance (two capacitors in parallel) in the same area and thus increase integration of dies. For example, the second IPDiA capacitor in the table has an area four times smaller than the first one but a capacitance ten times smaller.

### Capacitance Analysis Table

<table>
<thead>
<tr>
<th>Mfr</th>
<th>Capacitor</th>
<th>Capacitance</th>
<th>Size</th>
<th>Trenches Depth</th>
<th>Trenches area on the Die</th>
<th>Layers of Polysilicon</th>
<th>Capacity density</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPDiA</td>
<td>935121427710-T1N</td>
<td>1µF</td>
<td>xxx mm²</td>
<td>xx µm</td>
<td>xxx mm²</td>
<td>2</td>
<td>xxx µF/mm²</td>
</tr>
<tr>
<td>IPDiA</td>
<td>935121425610-T3N</td>
<td>0,1µF</td>
<td>xx mm²</td>
<td>xx µm</td>
<td>xxx mm²</td>
<td>2</td>
<td>xxx µF/mm²</td>
</tr>
<tr>
<td>IPDiA</td>
<td>935121424410-T3N</td>
<td>1000 pF</td>
<td>xx mm²</td>
<td>xx µm</td>
<td>xxx mm²</td>
<td>1</td>
<td>xxx µF/mm²</td>
</tr>
</tbody>
</table>

**Schematic representation of the IPDiA capacitor structure with two layers of polysilicon**

**Schematic representation of the IPDiA capacitor structure with one layer of polysilicon**
In this report, we simulate a production using 6 inches (150mm) wafers.

**Capacitor wafer fab unit:**
- Name: IPDiA Caen
- Wafer diameter: 6” (150mm)
- Capacity: 12 500
- Year of start: 1989
- Most advanced process: Silicon Deep Etching & Low Pressure Chemical Vapor Deposition
- Products: IPDs
- Location: 2 Rue de la Girafe, Caen, France

We assume a post depreciation rate of 25% for clean-room and equipment.
Capacitor Process Flow IPDiA (0402)

Capacitor Wafer Process:

The manufacturing of the IPDiA 935121424410-T3N(0402) follow the Patents “US 9, 647, 057 B2” and “US 8, 283, 750 B2” too, but it only has one layer of polysilicon, it explains its low capacitance:

- Beginning with the hole etching of the trench capacitors.
- The substrate is doped by a ion implanter followed by a thermal step which finishes the diffusion
- The dielectric is deposited
- First layer of polysilicon is deposited
- Insulate layer of oxide is deposited between polysilicon and aluminum
- Metal layer 1 is deposited to realize connection between polysilicon & doped silicon
Yields Explanation

The wafers and dies are tested during the process flow. There are 2 types of test:

The tests on the physical characteristics of the wafer like the thickness deposited.

The tests on the electrical functionalities of the die.

The difference is important because with the physical test, a bad result means a problem on a step and all the dies on the wafer are defective, so the wafer is scrapped. Usually these yields are good for mature technologies.

The tests on the dies are different. Each die is tested, one by one or simultaneously using “parallel” tests, and only the defective dies are scraped. During the probe test which is realized on the wafer, the defective dies are marked and are not assembled in package.

<table>
<thead>
<tr>
<th>Process</th>
<th>Yield</th>
<th>Apply on</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front-End</td>
<td>Manufacturing Yield</td>
<td>Die</td>
<td>The defective wafers are scraped</td>
</tr>
<tr>
<td>Back-End 0</td>
<td>Probe yield</td>
<td>Die</td>
<td>The defective dies are scraped. The number of good dies is function of the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>probe yield. Only the good dies are assembled in the package</td>
</tr>
<tr>
<td>Back-End 0</td>
<td>Dicing Yield</td>
<td>Die</td>
<td>The defective dies are scraped</td>
</tr>
<tr>
<td>Back-End 0</td>
<td>Thermal Probe Test</td>
<td>Die</td>
<td>The components received a thermal treatment and they are probe tested.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Defective components are scraped</td>
</tr>
</tbody>
</table>
IPDiA Cost Analysis – Main steps

- Trench Capacitor Front-End Cost
- Probe Test Cost
- Dicing Cost

IPDiA LPSC Series
The main breakdown of the Front-End Cost is due to the **Equipment cost (xxxx%).**
The Die cost approximately $xxx.
The Front-End Cost represents xxx%, and the Yield losses xxxx%.
Yields Hypotheses

In our simulation, we assume a development and a production ramp up without important technical problem.
# Skyworks SC00380912 Front-End Step Cost

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Cost</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Material</td>
<td>$123</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Assembly</td>
<td>$234</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Testing</td>
<td>$345</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Packaging</td>
<td>$456</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Shipping</td>
<td>$567</td>
<td></td>
</tr>
</tbody>
</table>

## Cost Analysis
- Synthesis
- IPDiA Cost Analysis
- Vishay Cost Analysis
- Skyworks Cost Analysis
- TSMC Cost Analysis

## Selling Price Analysis

## About System Plus
Estimated IPDiA Prices (935121427710-T1N)

<table>
<thead>
<tr>
<th>IPDiA 935121427710-T1N (1206 1μF)</th>
<th>Cost</th>
<th>Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component cost</td>
<td>$0,222</td>
<td></td>
</tr>
<tr>
<td>IPDiA Gross Profit</td>
<td>$0,155</td>
<td>+41%</td>
</tr>
<tr>
<td>Component price</td>
<td>$0,377</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IPDiA Estimated (from Murata AR 2016)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gross margin</td>
</tr>
</tbody>
</table>

The component manufacturing costs approximately $xxxx according to medium yield provided by our costing tool.

The component selling price costs approximately $xxxx according to medium yield provided by our costing tool.
REVERSE COSTING ANALYSES - SYSTEM PLUS CONSULTING

MEMS & Sensors – Packaging

- TSMC Integrated Fan-Out (inFO) Package in Apple’s A10 Application Processor
- TSMC Deep Trench Capacitor Land-Side Decoupling Capacitor in Apple’s A10 Application Processor
Business Models Fields of Expertise

- Custom Analyses
  (>130 analyses per year)
- Reports
  (>40 reports per year)
- Costing Tools
- Trainings

Overview / Introduction
Company Profile & Supply Chain
Physical Analysis
Physical Comparison
Manufacturing Process Flow
Cost Analysis
Selling Price Analysis
About System Plus
  - Company services
  - Related reports
  - Feedbacks
  - Contact
  - Legal
Contact

Headquarters
21 rue La Noue Bras de Fer
44200 Nantes
FRANCE
+33 2 40 18 09 16
sales@systemplus.fr

Europe Sales Office
Lizzie LEVENEZ
Frankfurt am Main
GERMANY
+49 151 23 54 41 82
llevenez@systemplus.fr

America Sales Office
Steve LAFERRIERE
Phoenix
USA
laferriere@yole.fr

Asia Sales Office
Takashi ONOZAWA
Tokyo
JAPAN
onozawa@yole.fr

Mavis WANG
GREATER CHINA
wang@yole.fr

www.systemplus.fr