BCD Technology and Cost Review

Power Semiconductor report by Sylvain Hallereau
August 2017 – Version 1
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Executive Summary

• This comparative study has been conducted to provide insight on technology data for BCD technologies used in integrated circuits. The report includes the study of at least 23 BCD technologies from 12 manufacturers: Infineon, STMicroelectronics, Freescale, NXP, Analog Devices, Renesas, Denso...

• System Plus consulting has been performing reverse engineering and costing of a large variety of smartpower IC for more than 15 years, only the latest generations are presented in this report.

• The report includes a first part which explains the main evolutions in BCD components in recent years.

• The second part is a review of 23 BCD technologies from 12 manufacturers to give a broad overview of available technologies and the difference between the different manufacturers.

• The report includes a detailed description of each technology. All of these technologies have been physically analyzed and compared.

• This report focus on manufacturing cost. The report includes a description of each technology and a simulation of the wafer manufacturing cost. All of these technologies have been physically analyzed and compared. The estimated wafer price does not include IP costs.

• Another report covers the costs of these technologies.
# Foundry Technologies Summary

<table>
<thead>
<tr>
<th>Foundry Technologies Review</th>
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<tbody>
<tr>
<td><strong>Infineon:</strong></td>
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<tr>
<td>SMART6</td>
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<td>SPT9</td>
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<tr>
<td><strong>STMicroelectronics:</strong></td>
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<tr>
<td>BCD6s</td>
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<td>SOI-BCD6s</td>
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<tr>
<td>BCD8</td>
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<tr>
<td>VIPower M0-3</td>
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<td>VIPower M0-5</td>
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<td><strong>Elmos:</strong></td>
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<td>BCD 0.8µm</td>
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<td><strong>Bosch:</strong></td>
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<td>BCD6</td>
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<td>BCD8</td>
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<td><strong>NXP:</strong></td>
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<tr>
<td>A-BCD3 SOI</td>
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<td><strong>Freescale (now NXP):</strong></td>
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<tr>
<td>SMARTMOS8</td>
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<td>SMARTMOS10W</td>
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<td><strong>Texas Instruments:</strong></td>
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<td>LBC5</td>
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<td>LBC8</td>
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<td><strong>Linear Technology:</strong></td>
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<td><strong>Analog Devices:</strong></td>
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<td>BCD 0.5µm</td>
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<td><strong>Denso:</strong></td>
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<tr>
<td>SOI-BCD 0.8µm,</td>
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<td>SOI-BCD 0.5µm</td>
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<td><strong>Renesas:</strong></td>
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<td>BCD0.15µm</td>
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<td><strong>Toyota:</strong></td>
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<tr>
<td>SOI-BCD 0.5µm</td>
</tr>
</tbody>
</table>
Synthesis

Synthesis of the 23 technologies/circuits analyzed in this report:

<table>
<thead>
<tr>
<th>Company</th>
<th>Technology name</th>
<th>Substrate</th>
<th>Technology node</th>
<th>Voltage Up to</th>
<th>metal layer</th>
<th>Alu / copper</th>
<th>Mask</th>
<th>Thick metal</th>
<th>Deep trench</th>
<th>Memory</th>
<th>Passive</th>
<th>Wafer Price</th>
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<tbody>
<tr>
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<td>SMART6</td>
<td>Silicon</td>
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<td>60V</td>
<td>2</td>
<td>Alu / Copper</td>
<td>17</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
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<tr>
<td>STMicroelectronics</td>
<td>BCD6s, SOI-BCD6s, BCD8s, VIPower M0-3, 5 and 7</td>
<td>Silicon</td>
<td>0.35µm</td>
<td>60V</td>
<td>2</td>
<td>Alu / Copper</td>
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<td>LBC5, LBC8</td>
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<td>Linear technology</td>
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<td>Analog Devices</td>
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**Overview / Introduction**

**Evolution of BCD Technologies**

**Foundry technologies Review**

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**About System Plus**
Overview / Introduction

Evolution of BCD Technologies
- Transistors
- Insulation
- Metal Layers
- Passive

Foundry technologies Review

About System Plus

About System Plus

**Transistor - Vertical DMOS**

STMicroelectronics ViPower XXX BCD process with vertical DMOS. The circuit integrates a vertical MOSFET. Similar to the planar MOSFET in discrete package.

The last generation of BCD IC with vertical transistor integrates trench power MOSFET to increase the current density.
Metal – Copper

Overview / Introduction

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Foundry technologies Review

About System Plus

Infineon SPT9 – 4 copper layers + a 5th Thick copper metal layer: cross-section SEM view
Infineon – SPT9 Transistors

- The process uses CMOS and LDMOS transistors
- Smallest length: ~XXµm
- The process should be XXXµm.
Infineon – SPT9 Wafer Cost Hypothesis

- We have chosen Infineon Dresden foundry in Germany, a 200mm wafer fab unit with 22,000 Wafers per month production capacity.

- This fab was founded in 1995.

- We assume that the clean-room and equipment depreciation is ended.

- We consider a residual depreciation of 25% for clean-room and equipment after the end of depreciation time.
Infineon – SPT9 Wafer Cost Breakdown

**Overview / Introduction**

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**About System Plus**

- Infineon – SPT9 Wafer Cost Breakdown

- The wafer cost is estimated at...

- With the Infineon gross margin, the wafer price is...
Related Reports

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- Industrial 100V MOSFET Technology and Cost Review
- Efficient Power Conversion EPC2040
- GaN Systems GaNpx Top Cooled – AT&S ECP® Embedded Power Die Package
- Transphorm TPH3002PS 600V GaN on Silicon HEMT
- GaN Systems – 650V GaN on Silicon HEMT AT&S ECP® Embedded Power Die Package
- EPC2010 GaN 200V power transistor
- Infineon – IPB60R280C6 600V CoolMOS C6 MOSFET
- Toshiba TK31E60W 4th gen DTMOS 600V Super-Junction MOSFET

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Manufacturing Process Flow
Cost Analysis
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