Sony IMX400 Tri-Stacked Image Sensor

First stacked CIS with Logic, Memory and sensing die

IMAGING report by Stéphane ELISABETH
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Executive Summary

• This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the Sony IMX400.

• This innovative CIS will be the next generation from Sony. The CIS included a 22 Mpixels array, a 1Gb DRAM die and a Digital Signal Processing on the same die footprint. This is the first tri-layers stacked CIS that we can find on the market. In this configuration, Sony can provide a fast readout image sensor with no distortion when shooting fast-moving object thanks to the high capacity DRAM between the Pixel Array circuit and the DSP circuit.

• Using the Sony’s Exmor-RS and the Xperi’s Zibond technology, Sony managed to integrate the three dies in a single thin, small and cost-effective die sensor. Surprisingly, the die sensor a unique sort of TSV with multiple level to interconnected the dies.

• This report includes a complete analysis of the Camera module from the Sony Xperia™ XZs, featuring camera module disassembly and die analyses, processes and cross-section. It also includes a comparison with Samsung Galaxy S7, Apple iPhone 7 Plus, and Huawei P9 telephoto camera modules. At the CIS level, it compares the IMX260, the IMX286, and the latest custom CIS for Apple from Sony’s portfolio. Finally, it contains a complete cost analysis and a selling price estimation of the CIS die.
Synthesis of the Physical Analysis

CIS Die:
- Dimensions:
- Optical Features:
- Electrical Connections and support:
- TSVs

Pixel Array Circuit:
- Process:
- Electrical Connection:
- Placement in the Module: Top on DRAM Die.

DRAM Circuit:
- Process:
- Electrical Connection:
- Placement in the Module: Mid between Pixel Array and Logic Die.

Logic Circuit:
- Process:
- Electrical Connection:
- Placement in the Module: Bottom beneath DRAM Die.
Physical Analysis Methodology

• Module is analyzed and measured.

• The module is opened to get overall dies data: dimensions, main characteristics, device markings.
  o Pictures of selected area are made in order to understand the connections of the CIS.
  o Cross section of Module to measure thicknesses and understand the assembly

• The CIS is separated to get overall die data: dimensions, main blocks, pad number and pin out, die marking.
  o Removal of metal layers (step by step) to identify the dies and measure the minimum dimensions.
  o Pictures of selected areas to identify the nature of the transistors.
  o SEM photographs to measure the transistors dimensions.
Module with Flex View & Dimensions

- Dimensions:
- Marking:

Module Top View

Module Bottom View

Module Side View

5.84 mm

Marking

©2017 System Plus Consulting | Sony IMX400 – Tri-layer Stacked CIS
Module Opening – Plastic Filter

• Plastic Filter dimension:
CIS Die – View & Dimensions

Physical Analysis
- Synthesis
- Module
- Module Cross-Section
  - CIS Die
  - CIS Cross-Section

Physical Comparison

Manufacturing Process Flow

Cost Analysis

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CIS Die – DRAM

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CIS Die Cross-Section

CIS Die Thickness:

- [ ]
- [ ]
- [ ]
CIS Die Cross-Section – Pixel Array

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CIS Die Cross-Section – Pixel Array/DRAM Bonding
CIS Die Cross-Section – TSVs Recap.
History of Sony’s CIS – TSVs

Sony XZs – TSVs Cross-Section View

Samsung Galaxy S7 – TSVs Cross-Section View

At Scale

Apple iPhone 6S – TSVs Cross-Section View

Huawei P9 – TSVs Cross-Section View
Global Overview

- Pixel Array
- DRAM
- Logic

Pixel Array Circuit with Microlenses

- CIS Die
- TSVs
- Logic Circuit
- DRAM Circuit
- Silicon Substrate

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DRAM/Logic Circuit Bonding Process Flow

Wafer Bonding

Lithography steps:
Pixel Array/DRAM/Logic Circuit Bonding Process Flow

Wafer Bonding

Lithography steps:
The **front-end cost** for the Logic circuit ranges from according to yield variations.

The largest portion of the manufacturing cost is due to the

We estimate a for the foundry supplier which result in a front-end price ranging from This correspond to the selling price to Sony.
### CIS Wafer & Die Cost

<table>
<thead>
<tr>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
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<tr>
<td>Logic Front-End Price</td>
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<tr>
<td>DRAM Front-End Price</td>
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<tr>
<td>Pixel Array Front-End Cost</td>
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<td>BSI &amp; TSVs Front-End Cost</td>
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<tr>
<td>CF + Spacer + ML Front-End Cost</td>
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<tr>
<td>BE : Probe &amp; Optical Test Cost</td>
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<td></td>
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<tr>
<td>BE : Dicing Cost</td>
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</tbody>
</table>

**Total Wafer Cost**

**Nb of potential dies per wafer**

**Nb of good dies per wafer**

**Die Cost Breakdown (Medium Yield)**

- Logic Circuit Cost
- DRAM Circuit Cost
- Pixel Array Cost
- BSI & TSVs Cost
- CF + Spacer + ML Cost
- BE : Probe Test & Dicing Cost
- BE : Yield losses

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By adding the probe test cost and the dicing cost, the CIS wafer cost ranges from [ ] according to yield variations.

The number of good dies per wafer is estimated to range from [ ] according to yield variations, which results in a die cost ranging from [ ].
Component Cost

Die Cost Breakdown According to Yield Variation
Related Reports

- Lenovo Phab2Pro – Google Tango Project – Time of Flight
- Melexis Automotive 3D ToF
- Apple iPhone 7 Plus Rear Dual Camera Module

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- 3D Imaging and Sensing 2017
- Equipment and Materials for 3D TSV Applications 2017
- 3D TSV and 2.5D Business Update - Market and Technology Trends 2017

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Business Models Fields of Expertise

Custom Analyses
(>130 analyses per year)

Reports
(>40 reports per year)

Costing Tools

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