Sony IMX400 Tri-layer Stacked CMOS Image Sensor (CIS) with Integrated DRAM and DSP

A closer look at the impressive, industry-first, tri-layer stacked CIS

Sony leads the global CMOS Image Sensor (CIS) market, commanding more than a third share of the industry’s total revenue. And over the years, Sony has maintained its leadership by providing innovative CIS products for original equipment manufacturers like Samsung or Apple. In 2017, Sony as a smartphone designer decided to release in its flagship the latest and potentially the greatest innovation in the past decade of CIS manufacturing. Inside the Sony Xperia™ XZs and the XZ Premium, the latest Motion Eye™ can be found, with the new IMX400 CIS. This three-layer stacked CIS is made with the traditional pixel array and logic circuit on the same die, but also a 1Gb DRAM memory allowing slow motion at almost 960 frames per second.

This innovative CIS is Sony’s next generation technology. The CIS includes a 22 Mpixel array, a 1Gb DRAM die and a digital signal processor (DSP) on the same die footprint. This is the first tri-layer stacked CIS on the market. In this configuration, Sony can provide a fast readout image sensor with no distortion when shooting fast-moving objects thanks to the high capacity DRAM between the pixel array circuit and the DSP circuit.

Using Sony’s Exmor-RS and Xperi’s Zibond technologies, Sony has managed to integrate the three dies in a single thin, small and cost-effective sensor die. Surprisingly, the die sensor uses a unique sort of TSV at different levels to interconnect the dies.

This report includes a complete analysis of the camera module from the Sony Xperia™ XZs, featuring camera module disassembly and die analyses, processes and cross-sections. It also includes a comparison with the Samsung Galaxy S7, Apple iPhone 7 Plus, and Huawei P9 telephoto camera modules. At the CIS level, it compares the IMX400 with the IMX260, the IMX286, and the latest custom CIS for Apple from Sony’s portfolio. Finally, it contains a complete cost analysis and a selling price estimation of the CIS die.
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  ✓ Module opening: AF driver including hall sensor, lenses, filter
  ✓ Module cross-section: lenses, filter
• CIS Die analysis
  ✓ CIS die view and dimensions: pixels, pads
  ✓ CIS deprocessing
  ✓ CIS die cross-section: TSVs, pixels
  ✓ Die process
• Physical Analysis Comparison
  ✓ Module: Samsung Galaxy S7, Apple iPhone 7 Plus, Huawei P9
  ✓ CIS die area: Samsung Galaxy S7 (IMX260), Apple iPhone 7 Plus, Huawei P9 (IMX286)

Manufacturing Process Flow
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• CIS, BSI and TSV Process Flow

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• Supply Chain Description
• Yield Hypotheses
• Wafer Cost Analyses: Pixel Array with Microlenses, Color Filters, and Spacer, Logic Circuit, DRAM Circuit
  ✓ Front-end cost
• BSI & TSVs Cost Analysis
  ✓ BSI & TSVs wafer front-end cost
  ✓ BSI & TSVs cost by process step
• CIS Die Cost

Estimated Price Analysis

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