NXP SCM-iMX6Q RCP SiP
Fan-Out System in Package from nepes
Packaging report by Stéphane ELISABETH
June 2017
SOMMAIRE

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Estimated Manufactured Price

Company services
Executive Summary

This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the **NXP SCM-i.MX6 Quad**.

This complete, low power solution will be dedicated to Internet-of-Thing (IoT) in the next few years. The modules include the i.MX6-Quad application processor, MMPF0100 power management system, a 16 MB Flash memory and about 100 SMD component, all in a single package of less than 200 mm$^3$.

The system uses non-conventional packaging developed by Nepes. The components are in Epoxy Molding Compounds (EMC) on few layer of redistribution layers (RDL). To enabling Package-on-Package configuration with Micron’s SDRAM memory chip, a custom redistribution device called Via Frame is integrated in the SiP to allow the memory stacking on the SiP.

Powered by the NXP i.MX6 Quad application processor, the Single Chip Module (SCM), SCM-i.MX6Q is extremely power efficient – ideal to reduce the product time to market by eliminating high-speed memory design and significantly reducing overall design complexity of the CPU/PMIC/Memory subs-system. Thanks to the RCP packaging technology applied to SiP, NXP has realized a very small low-power and high performance complete solution.

This report includes a complete analysis of the SiP, featuring dies analysis, processes, and package cross-section. Finally, it contains a complete cost analysis and a selling price estimation of the system.
RCP SiP Packaging Process Flow

RCP SiP Assembly:
- [ ]
- [ ]
- [ ]

APE Die:
- [ ] Process:
- [ ] Placement:

PMIC Die:
- [ ] Process:
  - [x]
- [ ] Placement:

Flash Memory Die:
- [ ] Process:
  - [x]
- [ ] Placement:
Package View & Dimensions

- **Package:** SCM (Single Chip Module)
- **Dimensions:** 14 x 17 x 0.8 mm
- **Pin Pitch:** 0.65 mm

**Top Marking:**
- MSCMMX6QZ0K 08AB 04 YYCTFD1617H

**Bottom Marking:**
- KOREA C07A01
RX Views

Physical Analysis
- Synthesis
- Package
- RX Views
- Package Opening
- Package Cross-Section
- RCP SiP Process
- APE Die
- Flash memory Die
- PMIC Die

Physical Comparison

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

About System Plus
Package Opening

Overview / Introduction

Company Profile & Supply Chain

Physical Analysis
  o Synthesis
  o Package
  o RX Views
    Package Opening
  o Package Cross-Section
  o RCP SiP Process
  o APE Die
  o Flash memory Die
  o PMIC Die

Physical Comparison

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

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SAMPLE
Package Opening – Bumps & First RDL

- Measured Line/Space Width in Bottom view:
  - RDL
Package Cross-Section – RDL & Bumps

- Copper RDL Thickness:

- Measured Line/Space Width in Cross-Section:
Package Cross-Section – Via Frame

- **Via Frame Dimensions:**
  - **Pitch:**
  - **PCB Thickness:**
  - **Hole Diameter:**
  - **Line/Space width:**
Package Cross-Section – Via Frame

Physical Analysis
- Synthesis
- Package
- RX Views
- Package Opening
  - Package Cross-Section
  - RCP SiP Process
  - APE Die
  - Flash memory Die
  - PMIC Die

Physical Comparison
Manufacturing Process Flow
Cost Analysis
Selling Price Analysis
About System Plus
APE Die Dimensions

Die Overview – Optical View

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Physical Analysis
- Synthesis
- Package
- RX Views
- Package Opening
- Package Cross-Section
- RCP SiP Process
  - APE Die
  - Flash memory Die
  - PMIC Die

Physical Comparison

Manufacturing Process Flow

Cost Analysis

Selling Price Analysis

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PMIC Die Cross-Section – Transistors

PMIC Die Cross-Section – LDMOS Transistor

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Comparison with Separate Packaging Solution

Exiting Separate package Solutions

<table>
<thead>
<tr>
<th>Product</th>
<th>Packaging Area</th>
<th>Packaging Type</th>
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<tbody>
<tr>
<td>APE</td>
<td></td>
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<tr>
<td>SPI NOR</td>
<td></td>
<td></td>
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<tr>
<td>PMIC</td>
<td></td>
<td></td>
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<tr>
<td>Total</td>
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RCP Solution

Several SMT included

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<thead>
<tr>
<th>Product</th>
<th>Packaging Area</th>
<th>Packaging Type</th>
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</thead>
<tbody>
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<td>SCM</td>
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<tr>
<td>Total</td>
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</tbody>
</table>

iMX6 – Quad

SPI NOR Memory

PF0100

* Assuming 1 mm spacing between packaging on app board

SAMPLE
Comparison With PoP Solutions – Shinko’s MCeP
Comparison With PoP Solutions – TSMC’s inFO

- TSMC’s inFO min. Line/Space width:
- Nepes’s RCP SiP min. Line/Space width:
Packaging Process Flow (1/6)

- PCB Substrate

Manufacturing Process Flow
- Synthesis
- Front-End Process & Fabrication Unit
  - RCP SiP Process Flow

Cost Analysis

Selling Price Analysis

About System Plus
### APE Front-End Cost

<table>
<thead>
<tr>
<th>Front-End</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Raw wafer Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Consumable Cost</td>
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<td></td>
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<tr>
<td>Labor Cost</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yield losses Cost</td>
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</tr>
</tbody>
</table>

**APE Front-End Cost**

**Gross margin**

**Masks Set Depreciation**

**APE Front-End Price**

---

**APE Front-End Cost Breakdown (Medium Yield)**
## RCP SiP Packaging Cost

<table>
<thead>
<tr>
<th>Package Manufacturing Cost</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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<tbody>
<tr>
<td>Glass Carrier Cost</td>
<td>Cost</td>
<td>Cost</td>
<td>Cost</td>
</tr>
<tr>
<td>Clean Room Cost</td>
<td>Breakdown</td>
<td>Breakdown</td>
<td>Breakdown</td>
</tr>
<tr>
<td>Equipment Cost</td>
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<tr>
<td>Yield Losses Cost</td>
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<tr>
<td>Package Manufacturing Cost</td>
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<tr>
<td>Gross margin</td>
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<tr>
<td>Package Manufacturing Price</td>
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</tbody>
</table>

### Selling Price Analysis

- Synthesis
- Supply Chain
- Yield Hypotheses
- Front-End Cost & Wafer/Die Cost
- RCP SiP Packaging Cost
- Component Cost

### About System Plus

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## Component Cost

<table>
<thead>
<tr>
<th></th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td><strong>Reconstituted Wafer Cost</strong></td>
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<td></td>
</tr>
<tr>
<td><strong>RCP SIP Manufacturing</strong></td>
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<td></td>
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</tr>
<tr>
<td><strong>Total Wafer Cost</strong></td>
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<td></td>
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</tr>
<tr>
<td>Nb of potential dies per wafer</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Nb of good dies per wafer</td>
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<td></td>
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</tr>
<tr>
<td>APE Die Price</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMIC Die Cost</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Flash SPI NOR Die Price</td>
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<td></td>
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<tr>
<td>SMD Component Price</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Via Frame</td>
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<tr>
<td>RCP SIP Cost</td>
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<tr>
<td>Final Test</td>
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<tr>
<td>BE: Yield losses</td>
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<tr>
<td><strong>Die Cost</strong></td>
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<td></td>
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</tbody>
</table>
Component Cost Breakdown (Medium Yield)

- APE Die Price
- PMIC Die Cost
- Flash SPI NOR Die Price
- SMD Component Price
- Via Frame
- RCP SiP Cost
- Final Test
- BE: Yield losses

Component Cost
## Estimated Manufacturer Price

### Table: Cost & Price According to Yield Variation

<table>
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<tr>
<th>Component</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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<tr>
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<td>Component price</td>
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</tbody>
</table>

### Graph: SCM iMX6Q Cost & Price According to Yield Variation

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**Overview / Introduction**

- Company Profile & Supply Chain
- Physical Analysis
- Physical Comparison
- Manufacturing Process Flow
- Cost Analysis
- Selling Price Analysis
  - Definition of Prices
  - Manufacturer Financial
  - Manufacturer Price

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- SP16276 – Qualcomm Snapdragon 820 MCeP vs. Samsung Exynos PoP
- SP16290 – Apple A10 TSMC’s integrated Fan-Out

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- Equipment and Materials for Fan-Out Packaging 2017

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- Reports (>40 reports per year)
- Costing Tools
- Trainings

- Display
- LED
- Power
- IC & RF
- MEMS & Sensor
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