NXP SCM-i.MX6 Quad High Density Fan-Out Wafer-Level System-in-Package

The first ultra-small multi-die low power module with boot memory and power management integrated in a package-on-package compatible device for the Internet of Things

In several applications, System-in-Package (SiP) integration of several devices with a very small form factor has become a huge challenge. New markets like the Internet-of-Things (IoT) bring new system configurations looking for low power consumption but high performance. NXP has therefore brought in a tiny wafer-level SiP an application processor that has been well-proven in automotive applications, a power management integrated circuit (PMIC) and a boot memory based on flash technology. Its footprint is about half the size of a discrete implementation on standard PCB.

This complete low power solution will be dedicated to Internet-of-Things (IoT) applications for the next few years. The module includes the i.MX6-Quad application processor, MMPF0100 power management system, a 16MB Flash memory and about 100 surface mounted devices, all in a single package smaller than 200 mm³. This is the first multi die fan-out device than we have found in the market, and could be a key milestone for fan-out SiP technology.

The system uses non-conventional wafer-level packaging developed by Nepes. It has innovative interconnections, enabling a Package-on-Package (PoP) configuration with Micron’s SDRAM memory chip. A custom redistribution device, called Via Frame, allows memory stacking. These components are integrated in Epoxy Molding Compounds (EMC) on a few redistribution layers (RDL).

Powered by the NXP i.MX6 Quad application processor, the Single Chip Module (SCM), SCM-i.MX6Q is extremely power efficient. This makes it ideal to reduce product time to market by simplifying the high-speed memory design and significantly reducing the overall design complexity of the processor/PMIC/memory sub-system. Thanks to the redistributed chip packaging technology applied to this SiP, NXP has realized a complete, very small, low-power, high performance solution.

This report includes a complete analysis of the SiP, featuring die analyses, processes, and package cross-sections. It also includes a comparison with TSMC’s inFO and Shinko’s MCeP PoP technology. Finally, it contains a complete cost analysis and a selling price estimation of the system.
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