Fan-Out Packaging
Technologies and market trends

2016 Edition
The objectives of the report are to:

- Provide a commercialization status of current and future Fan-Out technologies and products using them
- Deliver an overview of key players and supply chain activities
- Provide market and unit forecasts for the next five years and predict future application trends
REPORT METHODOLOGY

Market forecast methodology

Application

- Forecast of system market volume (unit)
- Definition of functions using devices, technical requirements at device level and device penetration rate and competitiveness with alternative technologies
- Forecast of device market volume (unit)
- Definition of ASP per application
- Forecast of device market size ($)  
- Forecast of device manufacturing equipment and material markets (unit and $)
- Forecast of device substrate markets (unit, wafers and $)
- Definition of manufacturing flows for front-end and packaging at module and device level

Market segmentation methodology

USES
- Variant
- Quasi segments

APPLICATIONS

CLIENTS
- Commercial key success factors behaviour and competitor behaviour matrices

SEGMENTS

BEHAVIOUR

System Plus Consulting expertise in reverse costing / reverse engineering

Definition of device die surface (mm²) and substrate die surface (mm²) and epiwafer volume (unit)
Technology analysis methodology

- Define the key parameters
- Understand the requested specifications per parameter and application
- Define the competing technologies and the potential evolutions of the technologies
- Define the roadblocks and challenges to be overcome
- Establish the technology roadmaps and maps
- Experts discussions

Information collection

- Material makers
- Equipment makers
- Device makers
- System designers
- OSAT
- Analysts’ processing to answer your needs and questionnaires on market size, positioning, technical challenges...

- Trade shows attendance and participation
- Analysis of the literature, web, scientific publications, white papers...
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ABOUT THE AUTHOR

Biography & contact

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Jérôme Azémar is a member of the Advanced Packaging & Manufacturing team of Yole Développement, the “More than Moore” market research and strategy consulting company. Upon graduating from INSA Toulouse with a master’s in Microelectronics and Applied Physics, he joined ASML and worked in Veldhoven for three years as an Application Support Engineer, specializing in immersion scanners. During this time he acquired photolithography skills which he then honed over a two-year stint as a Process Engineer at STMicroelectronics. While with STMicroelectronics, he developed new processes, co-authored an international publication and worked on metrology structures embedded on reticles before joining Yole Développement in 2013.

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Report sample
**Fan-Out WLP Background**

Technology benefits over other packages

- **Fan-Out Wafer-Level-Packages offer advantages over common packages.**
  - Over flip-chip BGA:
    - Slightly smaller footprint (clearance distances to the edges are smaller)
    - No substrate/interposer → Shorter interconnections meaning higher electrical performance, lower cost and thinner package
    - Higher potential for SiP and 3D integration
    - Lower thermal resistance
  - Over fan-in WLCSP:
    - Higher board-level reliability
    - Fan-Out area can go beyond chip area limitation
    - Higher potential for SiP integration
    - Lower thermal resistance
    - Built-in back-side protection (That protection is available for WLCSP as an option only, see slides describing FIMP and Flex Line later in the report)

FOWLP has the potential to go beyond competing packages
FAN-OUT WLP KEY DIFFERENTIATORS

FOWLP provides several advantages

1. Smaller footprint and thinner package than Flip-Chip BGA
2. Lower thermal resistance compared to Flip-Chip BGA
3. Fan-out zone adaptable to customer needs
4. Shorter interconnections
5. Simplified supply chain and manufacturing infrastructure
6. No restriction in bump pitch
7. No laminate substrate required

And others such as:
- Better board level reliability compared to WLCSP
- RoHS and REACH compliant package
- Excellent electrical performance
- High degree of package design freedom
- Reliable, miniaturized high performance package
A lot of products are already packaged using Fan-In solution which is cheaper than Fan-Out. With die size reduction and higher pin count, manufacturers reach a limit of Fan-In feasibility and have two options:

- Reducing ball pitch in order to have more connections within the die surface.
- Going Fan-Out and allowing an easier redistribution.

Since pitch reduction is very challenging, Fan-Out approach is offering a good opportunity.

There are some specific applications in the mobile market where a very thin package is mandatory for small packages (1mm x 1mm) and chips embedded are so small that WLCSP is not possible but volume for these application is limited.
FAN-OUT WLP PRINCIPLE

Chips are embedded in a mold compound

- Tape lamination
- Pick and place
- Wafer level molding
- Carrier removal / de-bonding
- Standard WLB process (Passivation, pattern, RDL, bonding)
- Dicing
- Carrier with foil and chips
- Carrier (Metal)
- Molding with liquid mold compound
- Reconstituted wafer after molding
- WLP Fan-Out wafer
- After singulation

Source: Infineon

EMBEDDED PACKAGING TECHNOLOGIES

Embedded packaging technologies with connections fanned out from the IC surface

Embedding in organic laminate
- Lamination around the chip
- Cavity dig in substrate

Encapsulator type

Embedding in epoxy mold compound
- RDL
- Foundry BEOL
- Advanced Substrate
- CF / CL
- CF / CL
- CL
- FU / FD
- FU / FD

Process type

CHIP FIRST: CF
CHIP LAST: CL
FACE UP: FU
FACE DOWN: FD

Interconnections type

Chip placing

Chip orientation

Fan-Out scope

FAN-OUT WLP: TECHNICAL CHALLENGES

**Warpage**
Nonuniform stress during process steps like molding compound deposition and die placing can impact wafer flatness and stress on dies.

**Topography**
Due to different sizes of devices to embed, non planarity can become an issue for SiP integration.

**Chip-to-mold non-planarity**
Die protrusion at the interface can lead to RDL distortion.

**Reliability**
In case of large packages (beyond 20*20mm) creep fatigue and solder joints issues appear.

**Die shift**
Lack of precision in die positioning during pick and place induces challenges for lithography steps and alignments.

FOWLP features come with technical challenges, addressed in different ways by the manufacturers.
VOLUME PRODUCTION ROADMAP FOR FOWLP

Key parameters

Roadmap described here is for volume production and an average of the different technologies expected on the market.

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<th>2016</th>
<th>2017</th>
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<td>Minimum die-to-die distance</td>
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TECHNOLOGY ROADMAP FOR FOWLP

Different end-market applications roadmap

Current situation
- « Standard Fan-Out » spreading in automotive and medical apps
- « HD Fan-Out » existing only in Telecom market

Future Fan-Out
- « Standard Fan-Out » spreading to more complex applications to package (MEMS) and SiP
- « HD Fan-Out » to spread thanks to PoP/SiP and needs for integration

« High Density Fan-Out »
Area of interest

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<td>I/O counts</td>
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- ASICs and Sensors Arrays (MCP)
- Medical
- PMU/PMIC (MCP/SiP)
- Mixed Signal ASIC, RF
- Radar

Wearables (SiP)
Optics / MOEMS (SiP)
Automotive MEMS (SiP)
LEDs, Photonics (SiP)
M2M Communication

BioSensor (SiP)
Military/Space (SiP)
FAN-OUT VS. OTHER TECHNOLOGIES

A subtle trade-off between cost, performance and integration, case by case

Case study: Single Die Embedding
Best choice according to different drivers and parameters

Package <5x5mm²
Fan-Out
Fan-in
GPS, Audio Codec, etc…

Package 8x8mm²
Fan-Out

FC-BGA
PMU/PMIC, BaseBand, RF, etc…

Package >15x15mm²
Fan-Out
FC-BGA
APE, GPU, etc…
FAN-OUT VS. OTHER TECHNOLOGIES

A subtile trade-off between cost, performance and integration, case by case

Third case: PoP for APE
Where do we find Fan-Out? Some examples below

Orange: Devices that can be found in FOWLP packages today
Green: Devices that could be found in the future in FOWLP
Grey: Devices that will likely remain on WLCSP or flip-chip package or move to 3DIC or Embedded die
FAN-OUT TECHNOLOGIES HISTORY

Fan-Out history: A long development and the recent hype

Chip-first Face Down Fan-Out

Early Fan-Out suppliers (long history, high volume)

Chip-Last Fan-Out

Chip-first Face Up Fan-Out

Recent Fan-Out suppliers (« hype » followers, no high volume yet)

2006 - 2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017

RCP creation eWLB creation

eWLB licensing and first volume
RCP licensing and first volume
M-Series creation
RDL-First R&D

RDL-First R&D creation

InFO creation
InFO first volume

Many new technologies creation

2016 Fan-Out market status shows TSMC entry

2016: Apple A10 entry with TSMC InFO will change the Fan-Out market landscape!
FAN-OUT ACTIVITY MARKET FORECAST WITH APPLE ENTRY

Fan-Out activity revenues forecast (M$)
Breakdown by Fan-Out market type

Confirmation phase: Apple keeps its APE in FO and other players follow the trend

Apple/TSMC entry
CAGR ~ 30%

Transition phase
CAGR ~ 10%

CAGR ~ 80%

Intel Mobile/Infineon eWLB-driven
CAGR > 30%

"Core" Fan-Out "High Density" Fan-Out

$3 000M
$2 500M
$2 000M
$1 500M
$1 000M
$500M
$80M
$0M


~$2.5B

Fan-Out package shipments forecast
(Munits of 300 eq. wafers)

- Packages of 5x5 and 8x8 are the main contributors to Fan-Out market, being the sweet spot of that platform
- Large packages (>12x12mm²) represents the high-density Fan-Out used for APE and high IO counts applications. These applications will widespread in the future with Apple starting a trend.
FAN-OUT COST EVOLUTION: TRENDS FOR CARRIERS

Carriers in production and forecasts

Cost reduction pressure drives carrier size and carrier type reflection

Panels

Wafers

2009 - 2013  2015  2016  2017  2018  > 2018
ORDER FORM

BILL TO
Name (Mr/Ms/Dr/Pr):
Job Title:
Company:
Address:
City:
State:
Postal Code/Zip:
Country:
VAT ID Number for EU members:
Tel:
Email:
Date:

BY CREDIT CARD
Visa ○ Mastercard ○ Amex
Name of the Card Holder:
Credit Card Number: ________________________________
Card Verification Value (3 digits except AMEX: 4 digits): ___________
Expiration date: ____________ / ____________

BY BANK TRANSFER
BANK INFO: HSBC, 1 place de la Bourse,
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Bank code: 30056, Branch code: 00170
Account No: 0170 200 1565 87,
SWIFT or BIC code: CCFRFRPP,
IBAN: FR76 3005 6001 7001 7020 0156 587

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- Batteries / Energy Management
- Power Electronics
- LED
- Compound Semi.
- MEMS & Sensors
4 BUSINESS MODELS

- **Consulting and Analysis**
  - Market data & research, marketing analysis
  - Technology analysis
  - Strategy consulting
  - Reverse engineering & costing
  - Patent analysis

- **Financial services**
  - M&A (buying and selling)
  - Due diligence
  - Fundraising
  - Maturation of companies
  - IP portfolio management & optimization

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  - Market & Technology reports
  - Patent Investigation and patent infringement risk analysis
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  - Sample Preparation Automation Through Emerging Microfluidic Technologies
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  - Supply Chain Readiness for Panel Manufacturing in Packaging
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