Reverse Costing Analysis

TSMC Deep Trench Capacitor (DTC)
Land-Side Decoupling Capacitor in Apple A10 Application Processor

October 2016 – Preliminary Version – Written by Stéphane ELISABETH

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Executive Summary

• This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the **TSMC Deep Trench Capacitor** found in the Apple iPhone 7 Plus.

• Located under the inFO PoP, the Land-Side Capacitor (LSC) is in flip chip configuration and supported by an extra layer on the PCB.

• The LSC is a high density deep trench capacitor on silicon substrate developed by TSMC using trench capacitor to increase the capacitive area without changing the footprint of the component. Compared to MLCC technology, TSMC marked a huge breaking point with a component that can compete with ceramic capacitor.

• In this report, we show the differences and the innovations of this capacitor: trench silicon, oxide deposition, ... The detailed comparison with the LSC in the Exynos 8 and the Snapdragon 820 will give the pro and the cons of the TSMC’s LSC technology.

• Thanks to this LSC process, TSMC is able to propose a very thin capacitor, with a high density and same footprint as MLCC 0204. The result is a very cost-effective component that can compete with any ceramic capacitor. In the report, the cost comparison is also including in order to highlight the difference.
Apple iPhone 7 Plus Teardown

Apple iPhone 7 Plus Main Board (Top view)

A10 processor & baseband processor

1st part of RF components

2nd part of RF components & RF transceiver

Power managements IC & NFC

Wifi FEM and antenna modules
LSC Die Removal

Apple iPhone 7 Plus Main Board (Top view)

A10 processor & baseband processor

1st part of RF components
Package Views & Dimensions

- Package:
- Dimensions:
- Pin Pitch:

Package Side View
Die View & Dimensions

Die Overview

- Die area:
- Nb of PGDW per 8-inch wafer:
- Pads Number:

*PGDW*: Potential Good Die per Wafer
Die Process

Die Overview

DTC capacitor – SEM view

Return to TOC

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Die Cross-Section

Die Cut plan – Optical view

Die Cross-Section – SEM view

Source: Patent US
Deep Trench Capacitor – Process Flow (1/5)
### Wafer Front-End Cost

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<thead>
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<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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<tbody>
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<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
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<td>Clean Room Cost</td>
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<td>Labor Cost</td>
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<td>Yield losses Cost</td>
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<tr>
<td><strong>Front-End Cost</strong></td>
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**Die Front-End Cost Breakdown (Medium Yield)**

- Item 1
- Item 2

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### Die Cost

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<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
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<tr>
<td>Nb of potential dies per wafer</td>
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<td>Nb of good dies per wafer</td>
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**Front-End Cost**
- BE 0: Probe Test, Backgrinding & Dicing Cost
- BE 0: Yield losses Cost

### Die Cost Breakdown (Medium Yield)
## Estimation of the selling price

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<tr>
<td><strong>Die cost</strong></td>
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<tr>
<td><strong>TSMC Gross Profit</strong></td>
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<tr>
<td><strong>Manufacturer price</strong></td>
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**Cost & Price According to Yield Variation**

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• Reverse costing analysis represents the best cost/price evaluation given the publically available data, and estimates completed by industry experts.

• Given the hypothesis presented in this analysis, the major sources of correction would lead to a +/- 10% correction on the manufacturing cost (if all parameters are cumulated)

• These results are open for discussion. We can reevaluate this circuit with your information. Please contact us: