Thanks to TSMC, Integrated Passive Devices (IPD) are back in the mobile industry. Information about the Apple A10 application processor (AP) integrated into the firm’s latest flagship, the iPhone 7, mentions the use of the first PoP Wafer Level Packaging for consumer devices developed by TSMC, called integrated Fan-Out - Package-on-Package (inFO-PoP). But to enable this, TSMC has also integrated a brand new technology that has never been proposed before for high volume products. It is using high-density Deep Trench Capacitors (DTCs) on silicon substrates as land-side decoupling capacitors.

Located under the inFO-PoP, the Land-Side Capacitor (LSC) is in flip-chip configuration and supported by an extra layer on the printed circuit (PCB). The LSC has been developed by TSMC using trench capacitors to increase the capacitive area without changing the footprint of the component. This can compete with multilayer ceramic capacitor (MLCC) technology.

In this report, we show the differences from ceramic technology and the innovations of this capacitor, including the trench silicon, oxide deposition and electrical performances. The process is compared to IPDiA technology. Detailed comparison with the LSC in the Exynos 8 and the Snapdragon 820 APs will explain the pros and cons of TSMC’s LSC technology.

This DTC process enables TSMC to offer a very thin capacitor, with high density and the same footprint as a MLCC 0204 component. The result is very cost-effective, as comparisons with ceramic capacitors in this report will show.
Véronique is in charge of structure analysis of semi-conductors. She has a deep knowledge in chemical & physical technical analyses. She previously worked for 20 years in Atmel Nantes Laboratory. Stéphane Elisabeth Stéphane has a deep knowledge in materials characterizations and electronics systems. He holds an Engineering Degree in Electronics and Numerical Technology, and a PhD in Materials for Microelectronics. Yvon Le Goff (Lab) Yvon Le Goff has joined System Plus Consulting in 2011, in order to set up the laboratory of System Plus Consulting. He previously worked during 25 years in Atmel Nantes Technological Analysis Laboratory as fab support in physical analysis, and 3 years at Hirex Engineering in Toulouse, in a DPA lab.

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