Reverse Costing Analysis

Apple A10 with TSMC’s inFO Packaging
iPhone 7 Plus Application Processor

September 2016 – Version 1 – Written by Stéphane ELISABETH

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# Table of contents

**Glossary**

1. Overview / Introduction 4
   - Executive Summary
   - Reverse Costing Methodology

2. Company Profile 7
   - Apple Inc.
   - Apple Series Application processor
   - Fan-Out Packaging
   - TSMC Port-Folio
   - TSMC inFO packaging

3. Physical Analysis 15
   - Physical Analysis Methodology
   - iPhone 7 Plus Teardown 17
     - A10 Die removal
   - A10 Package-on-Package Analysis 23
     - A10 Package View, Dimensions
     - A10 Package XRay View
     - A10 Package Opening
     - A10 Package Marking
     - A10 Package Cross-Section
     - A10 Package Cross-Section – Adhesive & Passivation
     - A10 package cross-Section - TIVs
     - A10 package cross-Section – Solder Balls
     - A10 package cross-Section – RDL
   - Land-Side Decoupling Capacitor Analysis 48
     - Package View, Dimensions & Marking
     - LSC Package integration – Cross-Section
   - Package-on-Package Comparison 52
     - Packages Comparison Overview
     - Packages LSC comparison
     - Package comparison cross-section

4. Manufacturing Process Flow 70
   - Chip Fabrication Unit
   - Packaging Fabrication Unit
   - inFO Reconstitution Flow

5. Cost Analysis 81
   - Synthesis of the cost analysis
   - Main steps of economic analysis
   - Yields Hypotheses
   - Die Cost Analysis 86
     - Wafer Cost
     - Die Cost
   - inFO Packaging Cost Analysis 90
     - Packaging Wafer Cost
     - Packaging Cost per process Steps
   - Component Cost

6. Estimated Price Analysis 99
   - Manufacturer Financial Ratios
   - Estimated Selling Price

Contact 102
Executive Summary

- This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of iPhone 7 Plus Application Processors, the Apple A10.

- Located on the main board, the application processor (AP) (bottom package) and the DRAM Chip (top package) are in Package-on-Package (PoP) configuration. Depending on the version (iPhone 7 or iPhone 7 Plus), the DRAM memory has different space management.

- The Apple A10 is a Wafer-Level Package (WLP) using TSMC’s packaging technology with copper pillar as Through inFO Via (TIV) to replace the well-known Through Molded Via (TMV) technology. With this new technology, Apple marked a huge breaking point with the old traditional PoP found in the previous generations of his APs. In this report, we will show the differences and the innovations of this package: Copper Pillars, Redistribution layer, patent identification, silicon high density capacitor integration, … The detailed comparison with the Exynos 8 and the Snapdragon 820 will give the pro and the cons of the inFO technology compared to PoP packaging used in the market.

- Thanks to this inFO process, Apple is able to propose a very thin package on package, with a high number of I/O pads and better thermal management. The result is a very cost-effective component that can compete with any well-known PoP. In the report, the cost comparison is also including in order to highlight the difference.

- This report also includes a technical comparison with previous Apple AP, the A9.
Apple iPhone 7 Plus Teardown

- A10 processor & baseband processor
- 1st part of RF components
- 2nd part of RF components & RF transceiver
- Power managements IC & NFC
- Wifi FEM and antenna modules

Apple iPhone 7 Plus Main Board (Top view)

Apple iPhone 7 Plus Main Board (Bottom view)
A10 Package Views & Dimensions

- Package:
- Dimensions:
- Pin Pitch:

Package top view

Package bottom view

Package Side View
A10 Package Cross-Section

- Package total thickness (without balls):
  - Memory package thickness:
    - Memory dies thickness:
    - PCB thickness:
  - Processor package thickness:
    - Die thickness:
    - RDL thickness:

Package Cross-Section – Optical view (1)

PoP Package Cross-Section – Optical View
inFO package Process from TSMC

Source: Patent US

Copper Pillar Cross-Section – SEM view

- 
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Details Copper Pillar Cross-Section – SEM view
A10 package cross-Section – RDL

Package Cross-Section – Optical view (2)

Package RDL – Cross-Section – SEM View

Package RDL – Cross-Section – SEM View
Exynos 8 Package Cross-Section – Optical view

Snapdragon 820 Package Cross-Section – Optical view

Apple A10 Package Cross-Section – Optical view
**A10 Die Dimensions**

- **Die Area:**
- **Nb of PGDW per**
  - Assuming scribe line of 100μm
- **Pad number:**
## Wafer Front-End Cost

<table>
<thead>
<tr>
<th>Wafer Manufacturing 300mm</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
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<tr>
<td>Front End Cost</td>
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<tr>
<td>Masks set depreciation</td>
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<tr>
<td>Wafer Cost</td>
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<tr>
<td>Samsung Gross Margin</td>
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<tr>
<td>Wafer Price</td>
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</tbody>
</table>

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### Wafer manufacturing cost Breakdown (Medium Yield)

- [Diagram showing cost breakdown]

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## Die Cost

<table>
<thead>
<tr>
<th>Die Cost</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
</tr>
<tr>
<td>Wafer Price</td>
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<tr>
<td>Probe Test Cost</td>
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<tr>
<td>Backgrinding Cost</td>
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<tr>
<td>Dicing Cost</td>
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<tr>
<td><strong>Final Wafer Cost</strong></td>
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<tr>
<td>Nb of potential dies per wafer</td>
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<tr>
<td>Nb of good dies per wafer</td>
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<tr>
<td>Die Cost</td>
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</tr>
<tr>
<td>Probe Test, Backgrinding and Dicing</td>
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<tr>
<td>Yield losses</td>
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</tbody>
</table>

### Die Cost Breakdown (Medium Yield)

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- •
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### inFO Wafer Cost

#### Die Cost

<table>
<thead>
<tr>
<th>Yield</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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</thead>
<tbody>
<tr>
<td>Cost Breakdown</td>
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</table>

#### 300*300mm

<table>
<thead>
<tr>
<th>Component</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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</thead>
<tbody>
<tr>
<td>Cost Breakdown</td>
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<td></td>
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</tbody>
</table>
- Clean Room Cost
- Equipment Cost
- Consumable Cost
- Labor Cost
- Yield losses

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*Package Manufacturing Cost Breakdown (Medium Yield)*
## Component Cost

<table>
<thead>
<tr>
<th>Component Cost</th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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</thead>
<tbody>
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<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
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<tr>
<td>Dies Cost per Panel</td>
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<tr>
<td>Manufacturing Cost</td>
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<tr>
<td><strong>Final Panel Cost</strong></td>
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<tr>
<td>Nb of potential package per</td>
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<td>Die Cost</td>
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<td>Final Test Cost</td>
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<tr>
<td>Yield Losses Cost</td>
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<table>
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<th></th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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</thead>
<tbody>
<tr>
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<tr>
<td>Gross profit</td>
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<tr>
<td>Manufacturer price</td>
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</table>

Cost & Price According to Yield Variation
Reverse costing analysis represents the best cost/price evaluation given the publically available data, and estimates completed by industry experts.

Given the hypothesis presented in this analysis, the major sources of correction would lead to a +/- 10% correction on the manufacturing cost (if all parameters are cumulated).

These results are open for discussion. We can reevaluate this circuit with your information. Please contact us: