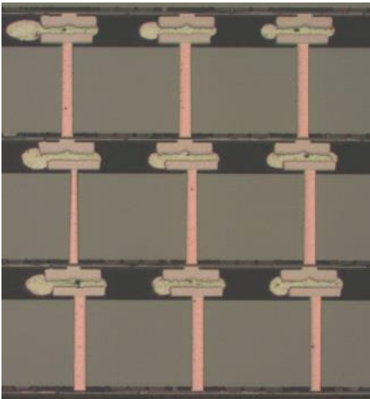
Samsung 3D TSV Stacked DDR4 DRAM

The First Memory product with Via-Middle TSV!



3D TSV technology is expected to reach $4.8B in revenues by 2019, mainly driven by 3D stacked DRAM and followed by 3D Logic/Memory and Wide I/O according to Yole Développement. With 40% share in the DRAM market, Samsung is by far the number 1 player. By introducing 3D TSV stacking in their latest 64GB DDR4, Samsung allows this technology to enter in the main stream.

This registered dual Inline memory module (RDIMM) includes 36 DDR4 DRAM chips (ref. K4AAG045WD), each of which consists of four 4Gb DDR4 DRAM dies (Ref. K4A4G085WD). The chips are manufactured using Samsung's 20nm process technology and 3D TSV via-middle package technology.

As a result, the new 64GB TSV module performs twice as fast as a 64GB module that uses wire bonding packaging, while consuming approximately half the power.

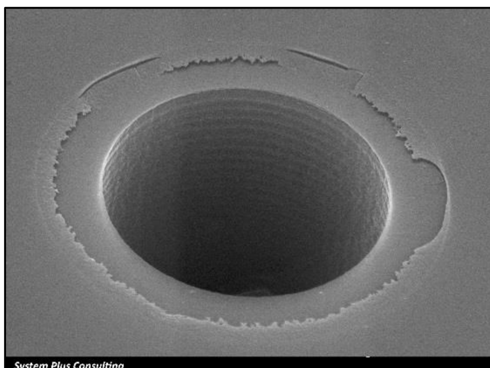
On the process side, Samsung used a temporary bonding approach using adhesive glue material and copper via-filled using bottom up filling. Also, System Plus paid particular attention in identifying all technical choices made by Samsung on process and equipment (wafer bonding, DRIE via etching, via filling, bumping, underfill…).

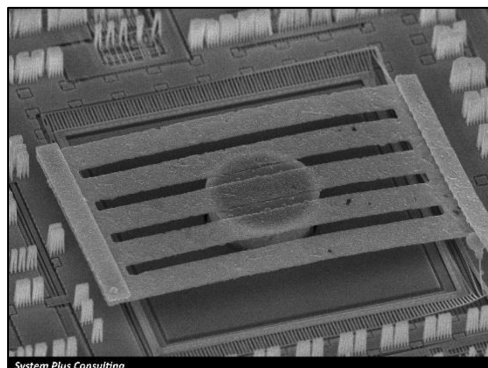
The report includes a complete physical analysis and cost estimation of the 3D packaging process, as well as a detailed description of the manufacturing process.

Title: Samsung 3D TSV
Pages: 100
Date: July 2015
Format: pdf + xls

COMPLETE TEARDOWN WITH:

- Detailed Photos
- Precise Measurements
- Material Analysis
- Manufacturing Process Flow
- Supply Chain Evaluation
- Manufacturing Cost Analysis
- Selling Price Estimation





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Romain is in charge of costing analyses for MEMS, IC and Advanced Packaging. He has published more than 50 Reverse Costing reports on various MEMS devices including Inertial, Pressure, Microphones or RF Sensors.

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		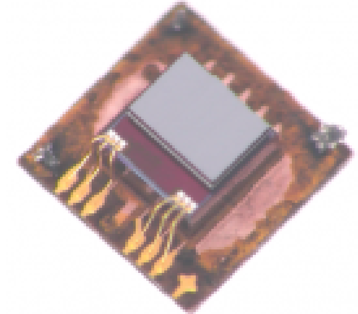
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