Reverse Costing Analysis

TDK-EPC P8009
PMU with MAXIM Embedded Dies

May 2013 – Version 1 – Written by Romain Fraux
# Table of contents

## Glossary

**1. Overview / Introduction** 4
- Executive Summary
- Reverse Costing Methodology

## 2. Companies Profile 8
- TDK-EPC Profile
- Maxim Integrated

## 3. P8009 Characteristics 13
- P8009 Characteristics
- P8009 Supply Chain

## 4. P8009 Physical Analysis 17
- Physical Analysis Methodology
- Module Views & Dimensions
- Passives Components & Functions
- Module Delamination
- MAX8955E – Die View, Dimensions & Marking
- MAX8955E – Die Process
- MAXQ6831 – Die View, Dimensions & Marking
- MAXQ6831 – Die Process
- Cross-Section 1 Overview
- Cross-Section 1 – Complete PCB
- Cross-Section 1 – Layer 1-2
- Cross-Section 1 – Layer 2-3
- Cross-Section 1 – Layer 3-4
- Cross-Section 2 Overview
- Cross-Section 2 – Shield Case
- Cross-Section 3 Overview
- Cross-Section 3 - MAX8955E
- Cross-Section 3 - MAXQ6831

## 5. Manufacturing Process Flow 58
- Global Overview
- MAX8955E Process
- MAXQ6831 Process
- ICs Wafer Fabrication Units
- SESUB Embedded Die Packaging Process Flow
- SESUB Panel Fabrication Unit
- Passives Assembly Process Flow

## 6. Cost Analysis 73
- Synthesis of the cost analysis
- Main steps of economic analysis
- Yields Hypotheses
- MAX8955E Front-End Cost
- MAX8955E Back-End 0 : RDL, Probe Test, Thinning & Dicing
- MAX8955E Die Cost
- MAXQ6831 Front-End Cost
- MAXQ6831 Back-End 0 : RDL, Probe Test, Thinning & Dicing
- MAXQ6831 Die Cost
- SESUB Panel Cost
- SESUB Panel Cost per process steps
- SESUB Panel : Equipment Cost per Family
- SESUB Panel : Material Cost per Family
- SESUB Panel : Panel Efficiency
- SESUB Packaging Cost per Module
- Passives Components Cost
- Passives Assembly Cost
- Back-End : Final Test Cost
- P8009 Module Cost & Price

## Contact 103

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• This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the **TDK-EPC P8009** component.

• The **P8009** is the first high volume Power Management Unit (PMU) using an embedded die packaging technology. The P8009 is integrated in some version of the BlackBerry Z10 and is targeted for TI OMAP4, nVidia TEGRA and Qualcomm Snapdragon platforms.

• The P8009 PMU is based on ICs from MAXIM Integrated: the MAX8955E PMIC (Power Management IC) and the MAXQ6831 16-bit RISC MCU.

• With a size of 11x11x1.6mm, the P8009 module achieves a size reduction of 60% compared to a discrete + BGA package solution.
Key Features:
- **Target Platform**: TI OMAP4 / nVidia Tegra / Qualcomm Snapdragon
- **Embedded IC**: MAXIM MAX8955E & MAXQ6831
- **5ch x 4.4 MHz Buck converters**
- **[1 x 2.6A and 1 x 2A for cores, 3 x 1.2A for IO etc.]**
- **High efficiency switch mode charger with Power Bypass Mode [up to 4A]**
- **Reverse Boost for Camera Flash LED (~2A) / USB OTG support**
- **1ch x high efficiency White LED back convertor, support 3-LED strings**
- **23ch x Low noise, high PSRR LDOs**
- **RTC with 32kHz crystal**
- **19.2/26.0MHz Clock generator with 5ch outputs (2 sinus, 2 square and 1 MP3)**
• Package is analyzed and measured.
• Package is opened in order to identify the elements constituting it.
• Cross-section are realized to get overall package data: dimensions, main characteristics.
• An analysis of the technologies and of the materials used is performed.
Module Views & Dimensions

- Package: SiP 380-bump BGA
- Dimensions: 11.0 x 11.0 x 1.6mm
- Ball pitch: 0.5mm
- Marking:
  - <logo Blackberry>
  - P8009Y938
  - 1227050011
  - E7
The shield case is soldered to the PCB substrate.

Module with shield soldered

Module with shield partially removed

Module with shield removed
Module Delamination – Layer 3

PCB layer 4

PCB Substrate after removing of layer 4 – Optical View

Pictures blurred in sample report
• The IC dies are embedded between the layer 3 and the layer 2.
• A redistribution layer is realized on top of the dies.

Layer 3 partially removed – Optical View

IC Dies Placement in the module – Optical View

(Pictures blurred in sample report)
MAXQ6831 – Die Process

- SRAM 6T Cell Size – SEM View
- SRAM 6T Memory – SEM View

- **Pictures blurred in sample report**

- SRAM 6T Memory is presents on the circuit.
  - Cell size:

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Cross-Section 3 - MAX8955E

- IC is thinned down to
- Copper redistribution layer (RDL) is realized on the IC die to ensure the connection with the metal layer of the PCB.
  - Copper RDL thickness
- Polyimide is used for the passivation layer.
  - Polyimide thickness:
Die embedding Process

- Solder mask (LPI deposition, exposure & developing)
- Board routing
- Electrical test
- OSP Finishing
- AOI inspection

Schematic Construction of the P8009 Module
### MAX8955E Die Cost

<table>
<thead>
<tr>
<th></th>
<th>Low Yield</th>
<th>Medium Yield</th>
<th>High Yield</th>
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<tbody>
<tr>
<td></td>
<td>Cost</td>
<td>Breakdown</td>
<td>Cost</td>
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<tr>
<td>FE : Wafer Price</td>
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<tr>
<td>BE 0 : Backgrinding Cost</td>
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<tr>
<td>BE 0 : Dicing Cost</td>
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<tr>
<td><strong>Final Wafer Cost</strong></td>
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<tr>
<td>Nb of potential dies per wafer</td>
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<tr>
<td>Nb of good dies per wafer</td>
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<tr>
<td>FE : Wafer Price</td>
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<tr>
<td>BE 0 : BG &amp; Dicing Cost</td>
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<tr>
<td>BE 0 : Yield losses Cost</td>
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<tr>
<td><strong>IC Die Cost</strong></td>
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</table>

- By adding the thinning cost and the dicing cost, the wafer cost ranges from... according to yield variations.
- The number of **good dies per wafer** is estimated to ranges from... according to yield variations, which results in a die cost ranging from...
### MAXQ6831 Front-End Cost

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<tr>
<td><strong>Breakdown</strong></td>
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</table>

- **Raw wafer (Si) Cost**
- **Clean Room Cost**
- **Equipment Cost**
- **Consumable Cost**
- **Labor Cost**
- **Yield losses Cost**

#### IC Front-End Cost

#### Foundry Gross Profit

#### IC Front-End Price

- **The front-end cost** for the MAXQ6831 ranges from [10000 to 20000] according to yield variations.
- **The largest portion of the manufacturer's cost** is due to the [30% to 40%]
- **We estimate a gross margin of [30% to 40%]** for the foundry, which results in a **front-end price ranging from [1000 to 2000]**
### SESUB Packaging Cost per Module

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<td><strong>SESUB Cost per Panel</strong></td>
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<tr>
<td>Nb modules per panel</td>
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<td><strong>SESUB Cost per module</strong></td>
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<tr>
<td>BE 1: Panel Efficiency</td>
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<td>BE 1: SESUB yield</td>
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- The SESUB packaging cost ranges vary according to yield variations.

*Pictures blurred in sample report*
### P8009 Module Cost

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<td>Passives Assembly Cost</td>
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<tr>
<td>Final test cost</td>
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<tr>
<td>Final yield losses</td>
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#### P8009 Module Cost Breakdown (Medium Yields)

- The P8009 module cost ranges from $X$ to $Y$ according to yield variations.
- The ICs manufacturing represents $Z$% of the module cost.
- The packaging (SESUB process) represents $A$% of the module cost.
- The passive components with the assembly represent $B$% of the module cost.
- Final test and yield losses account for $C$% of the module cost.

*Pictures blurred in sample report*
Reverse costing analysis represents the best cost/price evaluation given the publically available data, and estimates completed by industry experts.

Given the hypothesis presented in this analysis, the major sources of correction would lead to a +/- 10% correction on the manufacturing cost (if all parameters are cumulated)

These results are open for discussion. We can reevaluate this circuit with your information. Please contact us: