Reverse Costing analysis

eWLB (X-GOLD™ 213) by Infineon
Reverse analysis report of a Fan-out Wafer Level Package

January 2010- Version 1
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Physical Analysis Methodology

- Package is analyzed and measured.
  - X-ray pictures are used to identify the package construction and the redistribution.
- Two cross-sections are realized to get overall package data: dimensions, main characteristics.
- Analysis of the technologies and materials used is provided.

The schematic diagram below is constructed from observations made during this study and presented in the next slides.
Die in the package

This X-Ray picture of eWLB was taken after removal of the PCB.

- Die: 5.1mm x 5.1mm = 26.1mm$^2$
- Package: 8mm x 8mm = 64mm$^2$
- The fan-out ratio is 2.46 (package size over chip size)

The die is not centered in the package.
Some balls are right below the edge of the die and the fan-out area.
The back side of the wafer, after the wafer molding step, is grinded. It can be seen that the glass balls sealed within the mold compound were polished. A protective layer was deposited.

The filler content ratio is estimated at 75% of the Fan-Out mold compound. The high percentage of filler is necessary to obtain a low coefficient of thermal expansion (useful to limit the contraction of the reconfigured wafer at molding, and to match the silicon CTE).
Redistribution layer

Dielectric 2 : x.xx µm
Dielectric 1 : x.xx µm

Dielectric 2 : x.xx µm
Dielectric 1 : x.xx µm

We estimate at x.xx ml the necessary volume of dielectric for each layer per 8” wafer.
1) Wafer preparation: wafer thinning and sawing

2) Lamination of foil onto carrier

3) Pick, flip and placement of known good tested IC’s on foil

4) Wafer molding

5) Grinding of the epoxy resin (to release the stress difference between both sides so as to avoid wafer warping?)

6) Spin-on deposition of a back-side epoxy resin protection layer

7) De-bonding and foil removal, wafer is turned upside down, plasma cleaning and planarization of the front side

8) Application of a redistribution layer (1 seed layer deposition, 2 dielectric layers, 1 copper layer

9) Balling and singulation

Courtesy of

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eWLB – Fan-out package from Infineon
Fan-out wafer molding

- The carrier wafer is cleaned.
- An adhesive film is laminated onto the surface.

1. The dies are placed on the wafer with dots in a Fibonacci order.
2. The wafer is handled with a special glove. A container with the appropriate antistatic material is used.
3. The wafer stage is automatically cleaned in ultrasonic water.
4. The top side of the wafer is gridded to help remove the support. The wafer might be protected with a cover.
5. The front side of the wafer is cleaned to remove the support.
6. The wafer is automatically forced to remove the support. This step is optional. It continues until the edge of the wafer.
7. The wet etching is performed in the wafer for mask removal.
8. Wafer measurements are performed. Check the final states.
Wafer cost per Consumable Family for the medium cost scenario.

- Details of the material cost per step are given in the Excel Spreadsheet.
eWLB Wafer Cost

<table>
<thead>
<tr>
<th>Wafer cost breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scenario 1</strong></td>
</tr>
<tr>
<td><strong>Cost</strong></td>
</tr>
<tr>
<td>Depreciation Cost</td>
</tr>
<tr>
<td>Manufacturing Cost</td>
</tr>
<tr>
<td>Labor Cost</td>
</tr>
<tr>
<td><strong>STEPS COST</strong></td>
</tr>
<tr>
<td>Die cost</td>
</tr>
<tr>
<td>Yield Losses</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
</tr>
<tr>
<td>Manufacturing yield</td>
</tr>
</tbody>
</table>

- The main part of the wafer cost is due to the Manufacturing Cost: xx% in the “medium cost” version.
- The yield losses is a major cost factor, up to xx% for the “low yield” versions.
- The depreciation cost around xx% if new equipments are used (Scenarios 1 and 2).
- The labor cost is much higher in Germany (Sc. 1) but the overall weight is only xx%. 

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