Reverse Costing analysis

Texas Instruments
DLP® Pico™ projectors family
DLP® nHD, DLP® 0.3 WVGA, DLP® 0.17 HVGA

2012 September - Version 1
Written by: Maher Sahmimi

DISCLAIMER: System Plus Consulting provides cost studies based on its knowledge of the manufacturing and selling prices of electronic components and systems. The given values are realistic estimates which do not bind System Plus Consulting nor the manufacturers quoted in the report. System Plus Consulting is in no case responsible for the consequences related to the use which is made of the contents of this report. The quoted trademarks are property of their owners.

© 2012 by SYSTEM PLUS CONSULTING, all rights reserved.
# Table of Contents

1. Overview / Introduction .......................................................... 3
   - Executive Summary
   - Reverse Costing Methodology

2. Texas Instruments Company Profile ................................. 5

3. Physical Analysis ................................................................. 9
   - Synthesis of the Physical Analysis
   - DLP® 0.17 HVGA: Package Characteristics
   - DLP® 0.17 HVGA: Package Opening
   - DLP® 0.17 HVGA: Package Cross Section
   - DLP® 0.17 HVGA: Process technology
   - DLP® 0.17 HVGA: Micromirrors-Pictures
   - DLP® 0.3 WVGA: Package Characteristics
   - DLP® 0.3 WVGA: Package Opening
   - DLP® 0.3 WVGA: Package Cross Section
   - DLP® 0.3 WVGA: Process technology
   - DLP® 0.3 WVGA: Micromirrors-Pictures
   - DLP® nHD: Package Characteristics
   - DLP® nHD: Package Opening
   - DLP® nHD: Package Cross Section
   - DLP® nHD: Process technology
   - DLP® nHD: Micromirrors-Pictures
   - DLP®: Technology evolution

4. Manufacturing Process Flow .............................................. 79
   - Overview
   - CMOS Process Flow
   - MEMS Process Flow
   - Description of the Wafer Fabrication Units

5. Cost Analysis ................................................................. 88
   - Economic Analysis Hypotheses
   - Yields Explanation
   - Yields Synthesis
   - Synthesis of the Cost Analysis
   - CMOS Wafer Front-End Cost
   - CMOS Die Cost
   - MEMS Wafer Front-End Cost
   - MEMS Front-End Cost per Steps
   - MEMS Front-End Cost per Equipment
   - MEMS Front-End Cost per Consumables
   - MEMS Die Cost
   - Back-End: Package Cost
   - Back-End: Package Cost Per Steps
   - Manufacturing Cost

6. Estimated Manufacturer Price Analysis ....................... 135
   - Selling Price estimation
   - Estimated manufacturer Price

Contact
Glossary
Executive Summary

• This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of three TI DLP Pico projectors: DLP® nHD, DLP® 0.3 WVGA, DLP® 0.17 HVGA.

• The DLP® Pico™ devices are three MOEMSs (Micro-Opto-Electro-Mechanical Systems) designed by Texas Instruments and integrate an array of Micromirrors.

• The DLP® Pico™ nHD was extracted from the Galaxy beam phone. The component is packaged in a small ceramic housing (16mm x 6.9mm) and futures a nHD resolution (640 x 360).

• The DLP1700, features a Half-VGA Resolution (480 x 320), and has a 0.17-Inch Micromirror Array Diagonal, while the DLP3000 features a Wide-VGA Resolution (608 x 684) and has a 0.3-Inch Micromirror Array Diagonal. Both of them, were extracted from optima devices.
Reverse Costing Methodology

The reverse costing analysis is conducted in 3 phases:

- The dies are extracted in order to get overall data: dimensions, main blocks, pad number and pin out, die marking
- Set up of the manufacturing process.
- Setup of the manufacturing environment
- Cost simulation of the process steps with different year scenarios
- Supply Chain Analysis
- Analysis of the selling price
Physical Analysis
Optoma PK101: Teardown

Optoma PK101

AV Input Connector
LED Indicator
Lens
Focus Dial
Speaker

Top Cover
Main Board
Projector module

Optoma PK101: Teardown
DLP1700 : Package Characteristics & Marking

• **Package type**: Ceramic Land Grid Array CLGA

• **Package size**: 16mm x 9mm x 6mm

• **Pin pitch**: 0.6mm

The package marking includes:

8AA76Z0 012A

Plastic protection

Ceramic substrate

Back side with a Panasonic board to board connector
Ceramic substrate

Cross-Sectional Plane

Brazing with SiO2 spheres

Organic adhesive

Wall

DMD

Ceramic substrate

External pad used for the test.

Pad for the connector
Optoma PK301: Teardown

- Optoma PK301
- RGB LEDs
- Lens
- DLP3000
- Radiators
- Dichroic mirrors
- Pico DPP2600 ASIC/Processor

Texas Instruments – DLP® Pico Family
The package is a Ceramic Land Grid Array Package (CLGA)

Package Marking include:

- 2 9
- 145-1
- 07Z3J7A : Lot Trace Code
- 043B : Encoded Device Part Number
Galaxy Beam: Teardown

- Galaxy Beam
- Pico DPP2601 ASIC/Processor
- DLP nHD Projector module
- Fly’s-eye lens
- Dichroic mirrors
- Green LED
- Red & Bleu LEDs

© 2012 by SYSTEM PLUS CONSULTING, all rights reserved.

Texas Instruments – DLP® Pico Family
DLP nHD: Micromirrors Active Area

- Upper Address Electrode
- Mirror Control Bus
- Lower Address Electrode
- Springtip (cantilever flexure)
- Hinge (torsion flexure)
Manufacturing Process Flow & Cost Analysis
MEMS
- Oxide deposited
- CMP
- Pattern and etching via

MEMS
- Deposit tungsten, pattern and etch

MEMS
- Metal 3 (Al) deposit, pattern and etch
- Capping oxide deposit, pattern and etch

MEMS
- Sacrificial polymer deposit & pattern

Planarized Oxide

Tungsten

Capping Oxide

Aluminum

Sacrificial Polymer
## MEMS Wafer Steps Cost 1/2

<table>
<thead>
<tr>
<th>MEMS Front End</th>
<th>Cost</th>
<th>Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>10.7%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.0%</td>
</tr>
<tr>
<td>Planarized Oxide: Dry Etching Oxide</td>
<td>0.6%</td>
<td></td>
</tr>
<tr>
<td>Planarized Oxide: Photoresist Ashing</td>
<td>1.1%</td>
<td></td>
</tr>
<tr>
<td>Tungsten Plug: (Barrier) PVD-Titanium (Ti)</td>
<td>1.3%</td>
<td></td>
</tr>
<tr>
<td>Tungsten Plug: (Adhesion) PVD-Titanium</td>
<td>3.6%</td>
<td></td>
</tr>
<tr>
<td>Tungsten Plug: PVD-Tungsten (W)</td>
<td>3.4%</td>
<td></td>
</tr>
<tr>
<td>Tungsten Plug: Lithography single Side</td>
<td>1.2%</td>
<td></td>
</tr>
<tr>
<td>Tungsten Plug: Dry Etching tungsten</td>
<td>2.0%</td>
<td></td>
</tr>
<tr>
<td>Dark Metal M3: PVD-Titanium Nitride (TiN)</td>
<td>2.0%</td>
<td></td>
</tr>
<tr>
<td>Dark Metal M3: PVD-Aluminum (Al)</td>
<td>1.2%</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.9%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.6%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.4%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.4%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.9%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.6%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.6%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.7%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.8%</td>
</tr>
</tbody>
</table>
MEMS Wafer Consumables Cost

<table>
<thead>
<tr>
<th>Material Name</th>
<th>Material Cost</th>
<th>Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.3%</td>
<td>1.0%</td>
</tr>
<tr>
<td></td>
<td>0.5%</td>
<td>1.1%</td>
</tr>
<tr>
<td></td>
<td>1.0%</td>
<td>3.2%</td>
</tr>
<tr>
<td></td>
<td>4.1%</td>
<td>4.1%</td>
</tr>
<tr>
<td></td>
<td>4.1%</td>
<td>4.1%</td>
</tr>
<tr>
<td></td>
<td>4.6%</td>
<td>4.9%</td>
</tr>
<tr>
<td></td>
<td>5.0%</td>
<td>7.6%</td>
</tr>
<tr>
<td></td>
<td>7.7%</td>
<td>8.2%</td>
</tr>
<tr>
<td></td>
<td>8.9%</td>
<td>12.9%</td>
</tr>
<tr>
<td>SiH4</td>
<td>22.0%</td>
<td></td>
</tr>
</tbody>
</table>

Front End MEMS Material Cost Breakdown

- Photoresist: 22%
- TMAH: 13%
- SiH4: 9%
- DI Water: 8%
- Slurry Si: 8%
- O2: 8%
- Power: 5%
- HCl: 5%
- Ti/TiN Target: 4%
- Al Target: 3%
- C4F8: 3%
- SiCl4 SF6: 2%
- acetone: 2%
- C2F6: 1%
- Cl2: 1%
- Gaz: 1%
- 0%
• The reverse costing analysis represents the best cost/price evaluation given the publically available data, completed with industry expert estimates.

• Given the hypothesis presented in this analysis the major sources of correction would lead to a +/- 10% correction on the manufacturing cost (if all parameters are cumulated)
  - IC +/- 8%
  - MEMS +/- 5%
  - Test +/- 20%

• These results are open for discussion. We can re-evaluate this circuit with your information. Please contact us: