WHAT'S INSIDE

GaN HEMT transistor from EPC

Gallium nitride (GaN) Transistors' characteristics exceed those of conventional Si MOSFET or IGBT, as well as low Rds_{on}, higher current density and higher electron mobility.

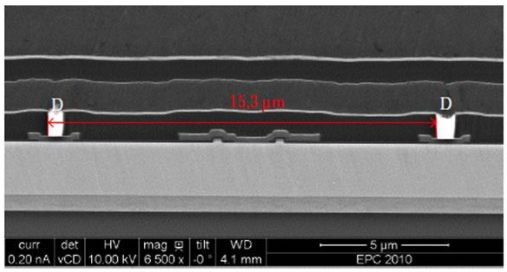
But up until now, the high cost of the bulk substrate - $1500 for a 2 - inch wafer - has prevented the adoption of GaN for power applications.

The economical solution proposed by Efficient Power Conversion Corporation (EPC), the first GaN transistor manufacturer, is called epitaxial technology: a GaN layer is deposited by epitaxy onto a low cost substrate, such as a six-inch silicon substrate.

Technology analysis

The HEMT transistors are manufactured at the surface of the substrate and are arranged laterally. The drain and source are on the top side, unlike silicon transistors which are built into the thickness of the substrate with the drain on the back side. This lateral arrangement minimizes the breakdown voltage of transistors and the current density.

Indeed, the pitch between the drain and source are a function of the breakdown voltage - we have observed a pitch of 7 µm for a transistor of 40 V and a pitch of 15.6 µm for a breakdown voltage of 200 V.



15.6 µm pitch for a 200 V transistor (Courtesy of System Plus Consulting)

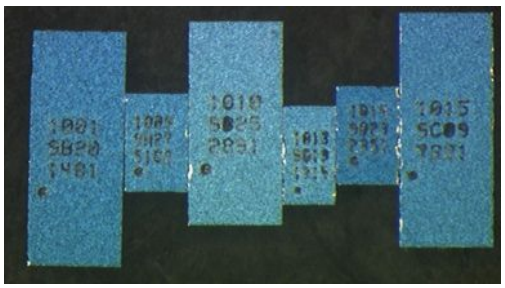
The current density of EPC's GaN transistors ranges from 5.35 A/mm² for a 40 V transistor to 2 A/mm² for a 200 V transistor.

All of EPC's GaN transistors are specified for medium voltages between 40 V and 200 V, and for a low Rds_{on} between 4 mΩ and 100 mΩ.

The first and second generation

All first and second generation transistors have a small area. The biggest transistor, 100 V, 25 A, is 6.56 mm², and the smallest is 1.53 mm².

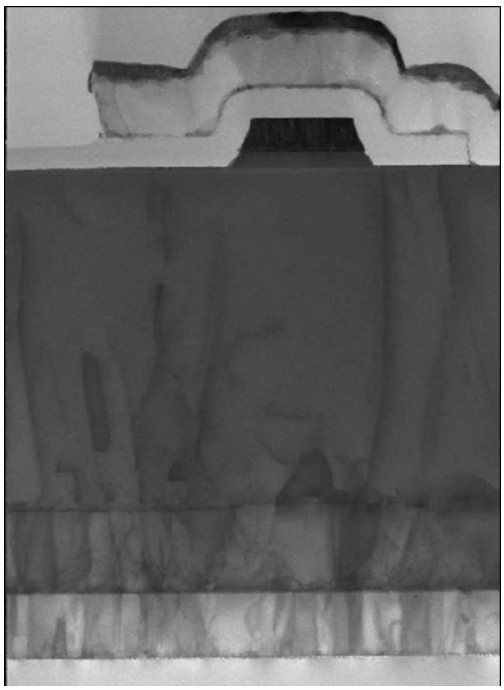
The absence of larger transistors is probably related to a highdefect density - The epitaxy defects limit the ability to produce larger transistors and stronger currents.



Six first-generation transistors (Courtesy of System Plus Consulting)

Thicker GaN epitaxial layer

The second-generation of transistors has an epitaxial layer twice as thick, which is likely to reduce the defect density at the surface. TEM analysis shows that the defect density is higher at the interface with the silicon substrate, and tends to be reduced nearer the surface.



TEM view of the GaN layer (Courtesy of System Plus Consulting)

By increasing the thickness of the GaN layer, EPC has reduced defects and improved manufacturing yields. This improvement should lead to the arrival of new, larger components in the future and thus higher currents as well as designs for higher voltage transistors.

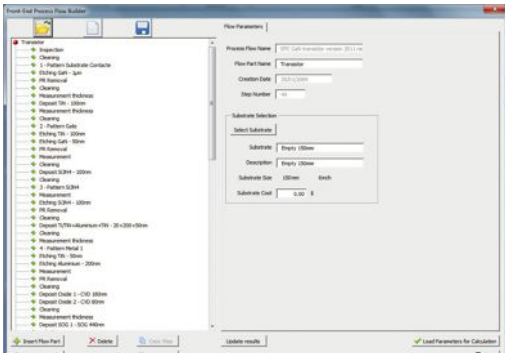
Wafer cost

Still, a thicker epitaxial layer means a higher manufacturing cost.

LED market driver cost reduction

Today, the GaN market is small and has limited funding for research - but it has benefited from the strong market growth of white LEDs. Indeed, the new high throughput epitaxy reactors developed for white LEDs and based on a GaN substrate are suitable for GaN transistors. Also, the price of raw materials such as TMAG has dropped due to the high volume of LEDs - in fact, the price of the GaN epitaxy step has halved over the last three years.

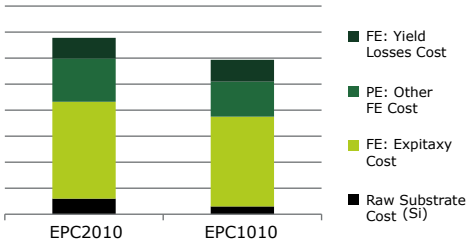
The wafer cost has been estimated using System Plus Consulting's Power CoSim+ costing tool (developed with MS-Excel™). Power CoSim+ is a powerful costing tool that allows manufacturers, designers and project leaders to calculate production costs and estimate the objective selling price of power electronics components.



Interface of Power CoSim+ (Courtesy of System Plus Consulting)

Ultimately, the cost of epitaxy has increased by only 15% between the first and second generation of EPC transistors, and represents almost 60% of the total. The final wafer price has increased by 10%.

Using the new analysis, along with the comments received on the first report, we have improved our assumptions of calculations for the second report of EPC's GaN transistors. The nature of the silicon substrate has been modified and the back-end process has been completed.



Wafer cost breakdown for between EPC2010 and EPC1010. (Courtesy of System Plus Consulting)

Conclusion

The design rules are not yet evaluated for the second generation of EPC transistors - only the epitaxy has been optimized. Productivity gains have helped to keep costs close, despite a thicker epitaxy. The new report explains the evolution in the technology of the GaN transistor of EPC.

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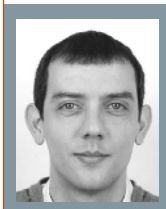

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He is in charge of costing analyses for Integrated Circuits, Power semiconductors and Packagings.

He has significant experience in the modeling of manufacturing costs for electronics components, and holds a Master of Microelectronics degree from the University of Nantes, France.