Texas Instruments' embedded die package

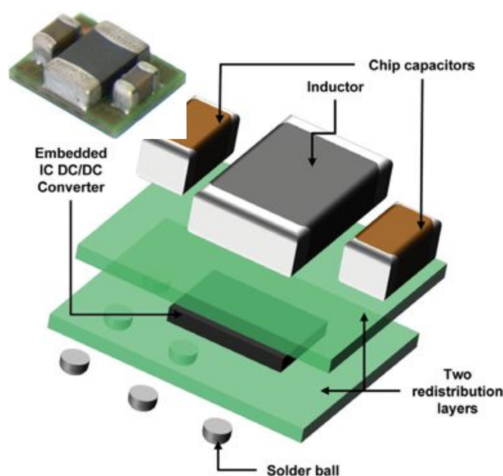
There continues to be strong demand for size reduction in mobile electronic products.

While fcCSP and WLCSP (fan-in and fan-out) are still showing impressive growth rates, embedded die packaging could be an interesting option for miniaturization and integration, especially since this is a native 3D-compatible technology.

Die embedding into PCB (Printed Circuit Board) laminated substrates has been developed by a wide range of companies for several years and in a variety of flavors - but Texas Instruments (TI) is the first to use this packaging technology in high-volume production.

Texas Instrument MicroSiP™

TI uses the MicroSiP™ designation for their modules which use embedded die packaging. The first components to use this packaging are TI's TPS8267x, high-frequency synchronous step-down dc-dc converters optimized for battery-powered portable applications. With dimensions of 2.9x2.3mm and an output current of 600mA, they provide a current density of 90mA/mm². Provided in an 8-pin, 1mm pitch bottom BGA interface, the modules include the DC-DC converter integrated circuit (IC), an inductor, and input/output capacitors.

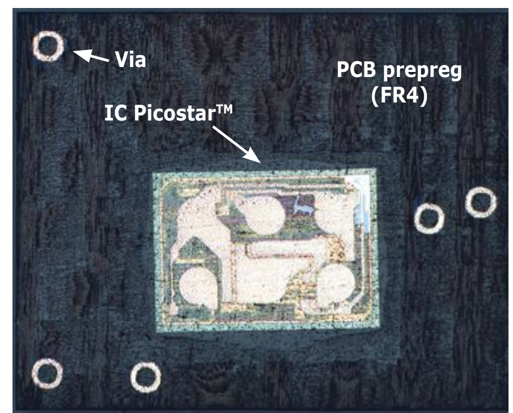


TI MicroSiP™ Module (Courtesy of System Plus Consulting)

TI Picostar™

The IC embedded in the MicroSiP™ module uses Texas Instruments' PicoStar™ package technology. The PicoStar™ is TI's die-sized package made by embedding the integrated circuit inside an HDI (High Density Interconnect) laminate substrate, and with a BGA balled surface area on the bottom face. The MicroSiP™ technology is just a superset of the PicoStar™ package type. A MicroSiP™ module can be built by mounting discrete passive components on the top surface of a PicoStar™ packaged IC, as is done for the TPS8267x product family.

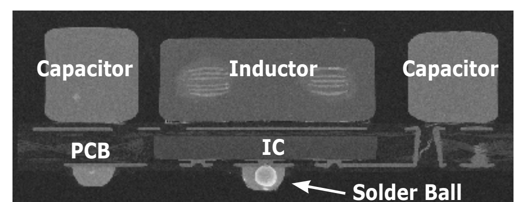
In this case, the IC is thinned down to 130µm and a copper redistribution layer (RDL) is patterned at the wafer level so as to distribute the pads over the die surface area, and prior to embedding the IC in the PCB laminate substrate.



MicroSiP™ Module Delaminated (Courtesy of System Plus Consulting)

AT&S ECP® process

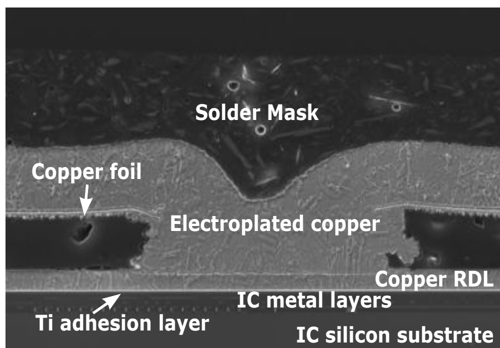
TI's PicoStar™ packages and MicroSiP™ modules use the Embedded Component Packaging (ECP®) process offered by AT&S, Europe's largest PCB manufacturer, and one of the world's top HDI PCB manufacturers. AT&S has invested years of R&D and specific equipment development in order to industrialize this technology. Most of the assembly operations are panel-scale operations—they are performed on AT&S's PCB infrastructure. They include the embedding process steps which provide the IC with a fan-out area and with 3D paths to both the top and the bottom sides of the embedding substrate. This packaging technology extends the package size beyond the IC surface area, and allows for the mounting of additional components such as discrete passives on top of the laminate SiP module.



MicroSiP™ Module Cross-Section (Courtesy of System Plus Consulting)

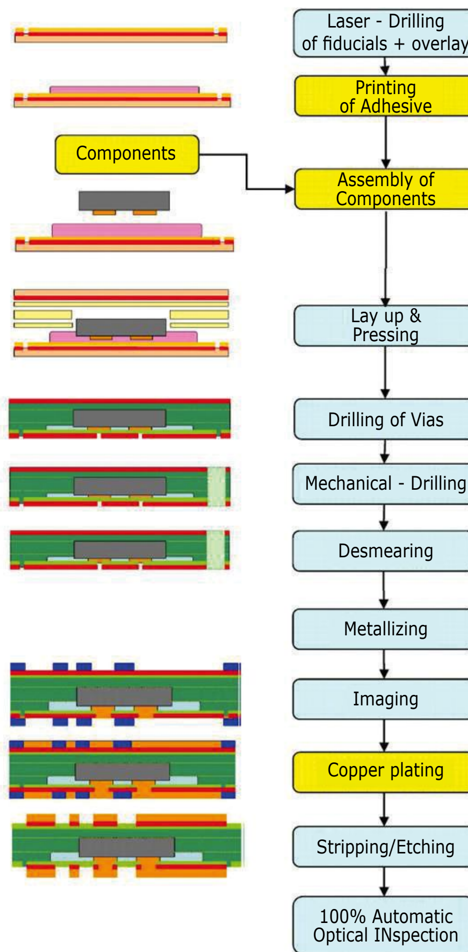
> **"Even if the total cost of ownership of this module is low enough for cost-obsessed consumer electronics applications, we think that the main driver is integration and miniaturization,"** explains Romain Fraux

The process begins with the realization of fiducials in a copper foil by laser drilling to define registration marks for mechanical process steps. Next, adhesive is screen-printed on the copper foil, and sawed and tested "known good dice" are placed with pick and place equipment. The adhesive is cured to ensure solid attachment to the copper foil. The IC is then embedded with a lamination process which presses together an FR4 prepreg with cavities for IC dies and a second copper foil. Through holes vias between the 2-sided PCB of ~150µm diameter are performed with a mechanical drilling process, and microvias enabling access to the IC pad through the bottom laminate layer of the embedded package are realized by laser drilling. Vias are then cleaned and metalized with electroless copper plating. The process to define the fine lines is realized with a semi-additive technology: photoresist is laminated on the copper foil, followed by the imaging process of the resist. The resist is developed and copper is electroplated in the non-covered areas of the resist. The semi-additive flow finishes with the stripping of the resist and the etching of the remaining exposed copper foil. The final steps consist of the formation of the solder mask, the finishing (OSP), and inspections and tests.



IC Pad connection Cross-Section (Courtesy of System Plus Consulting)

ECP® simplified process flow



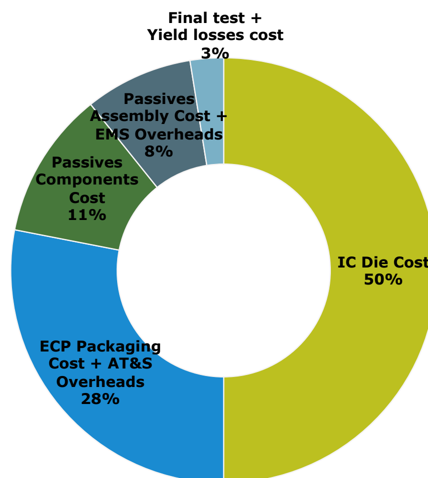
(Courtesy of AT&S)

Supply chain and cost structure

We believe that the manufacturing of the copper RDL on the device wafer and the mounting of the solder balls on the bottom surface of the package are realized by Texas Instruments themselves. The ECP packaging is currently done by AT&S on 18"x24" panels in Austria, allowing for assembly of more than 18,000 packages simultaneously. Specific steps of this packaging process flow (like placement of the ICs, laser drilling operations, and the semi-additive copper plating operations) require investments from AT&S, and they represent the bulk of the ECP packaging cost as of 2012.

Even if the total cost of ownership of this module is low enough for cost-obsessed consumer electronics applications, we think that the main driver is integration and miniaturization. By adopting this technology, TI spares its customers considerable development efforts, simplifies logistics and inventories, and saves on the application board space through this module approach.

MicroSiP module cost breakdown



(Courtesy of System Plus Consulting - March 2012)

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Romain Fraux is Project Manager for Reverse Costing analyses at System Plus Consulting. Since 2006, Romain is in charge of costing analyses of MEMS devices, Integrated Circuit and electronics boards. He has significant experience in the modeling of the manufacturing costs of electronics components. Romain has a BEng from Heriot-Watt University of Edinburgh, Scotland and a master's degree in Microelectronics from the University of Nantes, France.