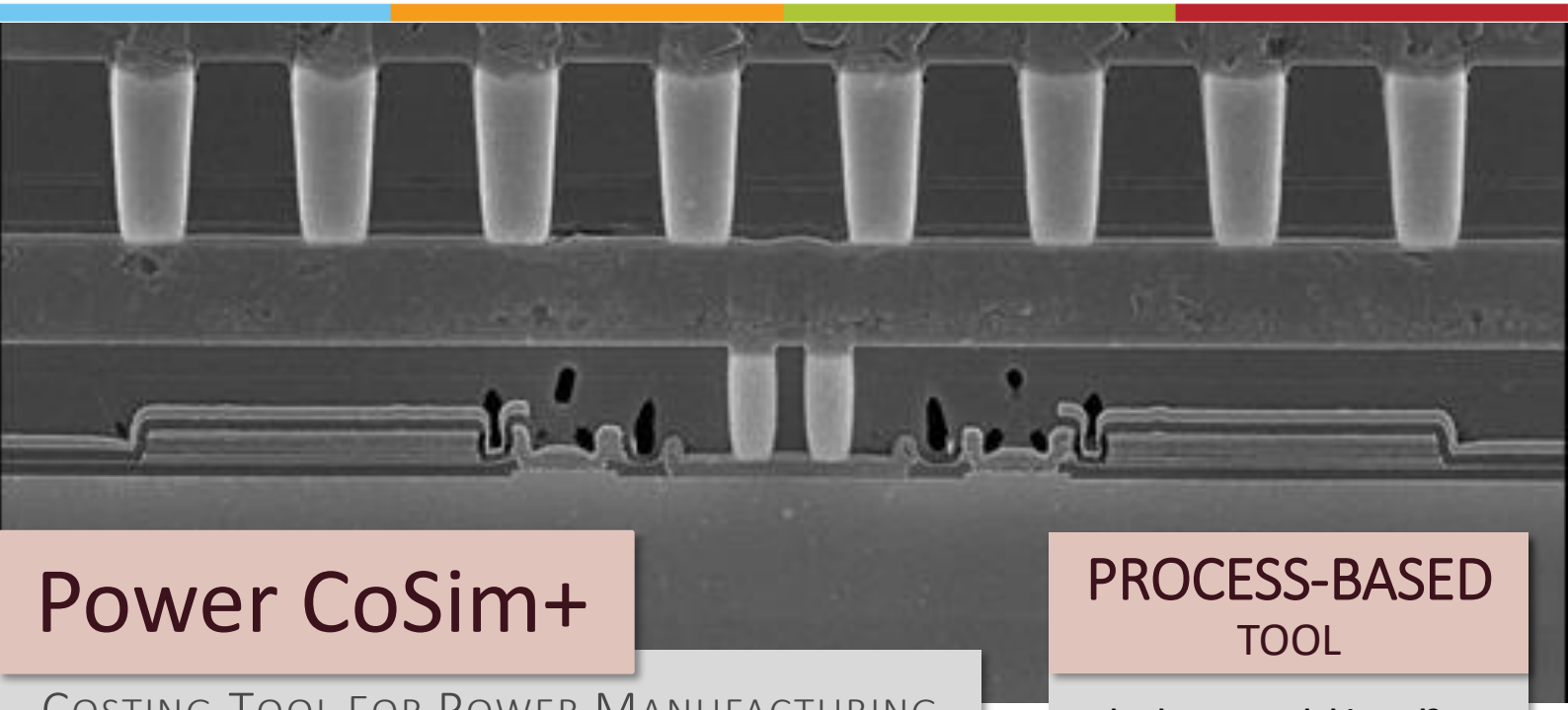
SYSTEMPlus CONSULTING

Reverse Costing & Technology Analysis TOOL



Power CoSim+

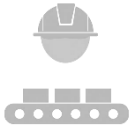
Costing Tool for Power Manufacturing

COMPLETE AND POWERFUL MANUFACTURING COSTING TOOL

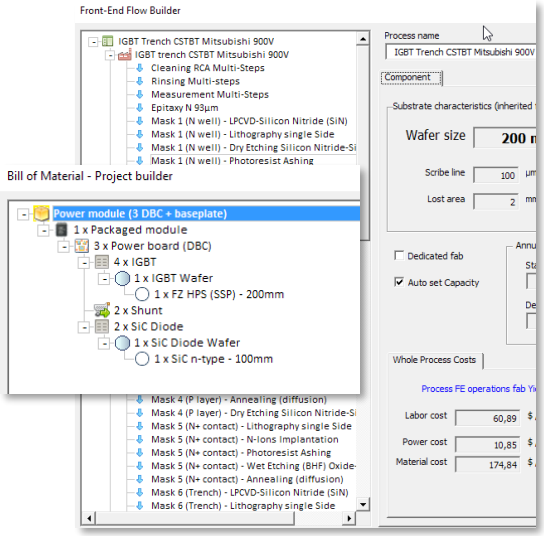
Due to their non-standard manufacturing processes, the power device costs can be difficult to estimate. Components such as superjunction MOSFETs, IGBTs and SiC diodes involve very different process steps.

Power CoSim+ is a flexible tool for evaluating the cost of any semiconductor process or power device, already used by manufacturers and end users.

With the possibility of storing steps and process flows in libraries, this new version dramatically reduces the duration of the cost evaluation.



Step by step, describe your process flow to get a detailed manufacturing cost analysis.



PROCESS-BASED TOOL

Why do you need this tool?

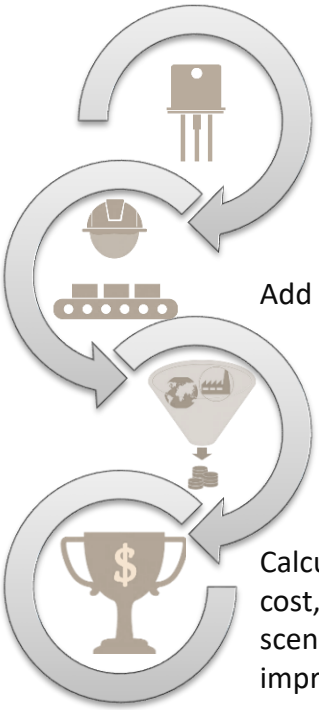
- Optimize your manufacturing cost
- Challenge your own production / process choices
- Create a business plan
- Change your fab and process
- Evaluate economic feasibility
- Simulate your equipment's operating cost

Who should buy this tool?

- Strategic marketing executives
- Process managers
- R&D engineers
- Power equipment suppliers
- Purchasing managers

POWER TYPES	PACKAGING	SUBSTRATES	TECHNOLOGIES	DATABASE
Diodes MOSFET, JFET IGBT, BJT Thyristor HEMT	Discretes Modules Embedded Molded	Silicon SiC GaN	Planar Trench Thin Film Compounds	Equipment Substrates Materials Wafer fab units Assembly units etc.

MAIN FEATURES



Describe the product

Add every process step

Enter the manufacturing location and supply chain

Calculate the manufacturing cost, compare up to 5 scenarios and choose improvements

Multiple process flows

Any power semiconductor process flow can be simulated with hierarchical description for multiple dies or processes, across an unlimited number of process steps or process flows.

Multiple conditions and supply chain

You can set up the tool with your own conditions, including location, clean room class, process type and subcontracting operation parameters.

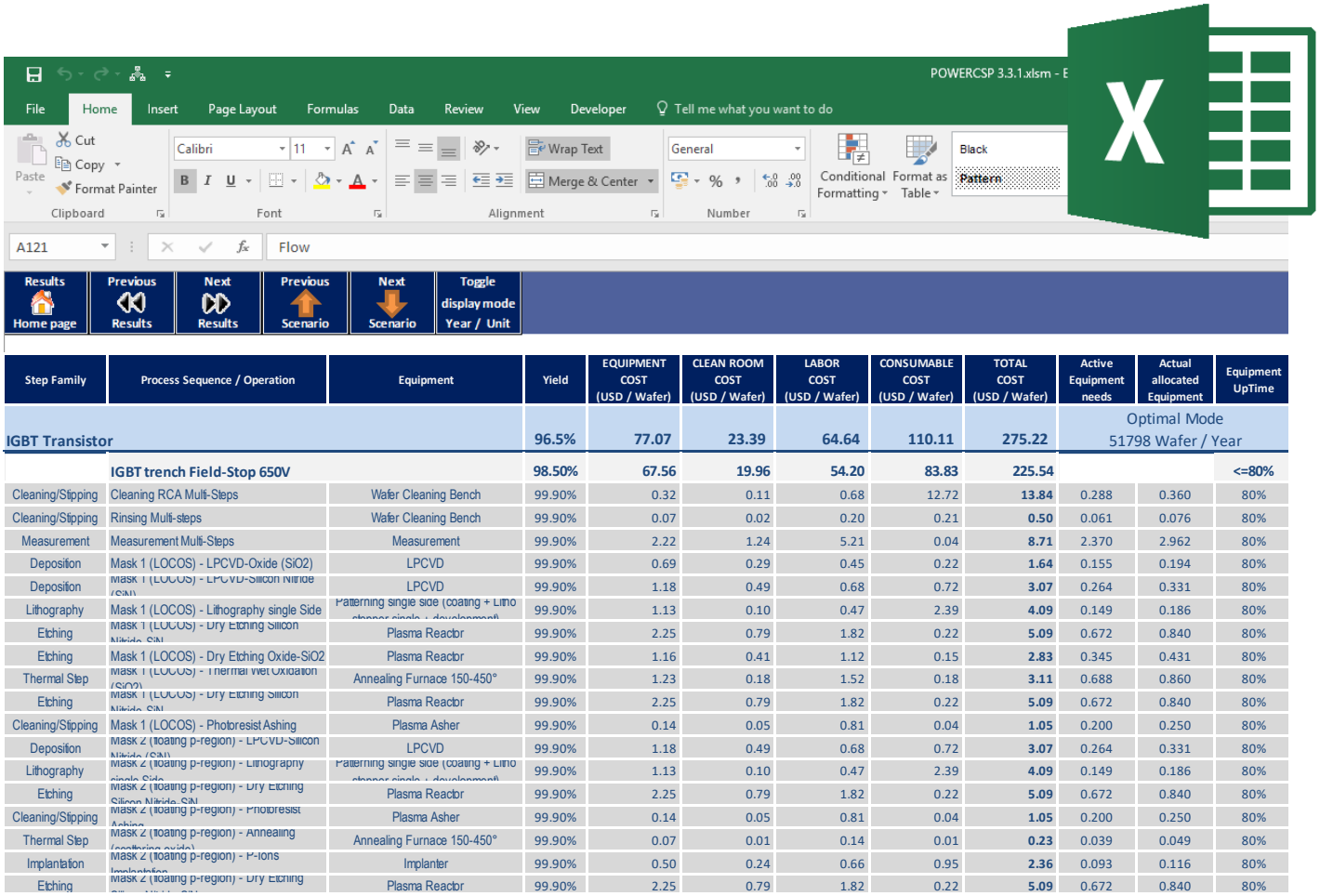
Results are fully open-format

Modify or export final results, build reports with any Excel workbook.

Safely workgroup-compliant

Secure multiple access, data sharing and data integrity.

Support and updates available



Step Family	Process Sequence / Operation	Equipment	Yield	EQUIPMENT COST (USD / Wafer)	CLEAN ROOM COST (USD / Wafer)	LABOR COST (USD / Wafer)	CONSUMABLE COST (USD / Wafer)	TOTAL COST (USD / Wafer)	Active Equipment needs	Actual allocated Equipment	Equipment UpTime
IGBT Transistor			96.5%	77.07	23.39	64.64	110.11	275.22	Optimal Mode 51798 Wafer / Year		
	IGBT trench Field-Stop 650V		98.50%	67.56	19.96	54.20	83.83	225.54			<=80%
Cleaning/Stipping	Cleaning RCA Multi-Steps	Wafer Cleaning Bench	99.90%	0.32	0.11	0.68	12.72	13.84	0.288	0.360	80%
Cleaning/Stipping	Rinsing Multi-steps	Wafer Cleaning Bench	99.90%	0.07	0.02	0.20	0.21	0.50	0.061	0.076	80%
Measurement	Measurement Multi-Steps	Measurement	99.90%	2.22	1.24	5.21	0.04	8.71	2.370	2.962	80%
Deposition	Mask 1 (LOCOS) - LPCVD-Oxide (SiO2)	LPCVD	99.90%	0.69	0.29	0.45	0.22	1.64	0.155	0.194	80%
Deposition	Mask 1 (LOCOS) - LPCVD-Silicon Nitride (SiN)	LPCVD	99.90%	1.18	0.49	0.68	0.72	3.07	0.264	0.331	80%
Lithography	Mask 1 (LOCOS) - Lithography single Side	Patterning single side (coating + Litho stepper single + development)	99.90%	1.13	0.10	0.47	2.39	4.09	0.149	0.186	80%
Etching	Mask 1 (LOCOS) - Dry Etching Silicon Nitride SiN	Plasma Reactor	99.90%	2.25	0.79	1.82	0.22	5.09	0.672	0.840	80%
Etching	Mask 1 (LOCOS) - Dry Etching Oxide-SiO2	Plasma Reactor	99.90%	1.16	0.41	1.12	0.15	2.83	0.345	0.431	80%
Thermal Step	Mask 1 (LOCOS) - Thermal Wet Oxidation (SiO2)	Annealing Furnace 150-450°	99.90%	1.23	0.18	1.52	0.18	3.11	0.688	0.860	80%
Etching	Mask 1 (LOCOS) - Dry Etching Silicon Nitride SiN	Plasma Reactor	99.90%	2.25	0.79	1.82	0.22	5.09	0.672	0.840	80%
Cleaning/Stipping	Mask 1 (LOCOS) - Photoresist Ashing	Plasma Asher	99.90%	0.14	0.05	0.81	0.04	1.05	0.200	0.250	80%
Deposition	Mask 2 (floating p-region) - LPCVD-Silicon Nitride (SiN)	LPCVD	99.90%	1.18	0.49	0.68	0.72	3.07	0.264	0.331	80%
Lithography	Mask 2 (floating p-region) - Lithography single Side	Patterning single side (coating + Litho stepper single + development)	99.90%	1.13	0.10	0.47	2.39	4.09	0.149	0.186	80%
Etching	Mask 2 (floating p-region) - Dry Etching Silicon Nitride SiN	Plasma Reactor	99.90%	2.25	0.79	1.82	0.22	5.09	0.672	0.840	80%
Cleaning/Stipping	Mask 2 (floating p-region) - Photoresist Ashing	Plasma Asher	99.90%	0.14	0.05	0.81	0.04	1.05	0.200	0.250	80%
Thermal Step	Mask 2 (floating p-region) - Annealing (oxidizing oxide)	Annealing Furnace 150-450°	99.90%	0.07	0.01	0.14	0.01	0.23	0.039	0.049	80%
Implantation	Mask 2 (floating p-region) - P-Ions Implantation	Implanter	99.90%	0.50	0.24	0.66	0.95	2.36	0.093	0.116	80%
Etching	Mask 2 (floating p-region) - Dry Etching Silicon Nitride SiN	Plasma Reactor	99.90%	2.25	0.79	1.82	0.22	5.09	0.672	0.840	80%

CONTACT

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