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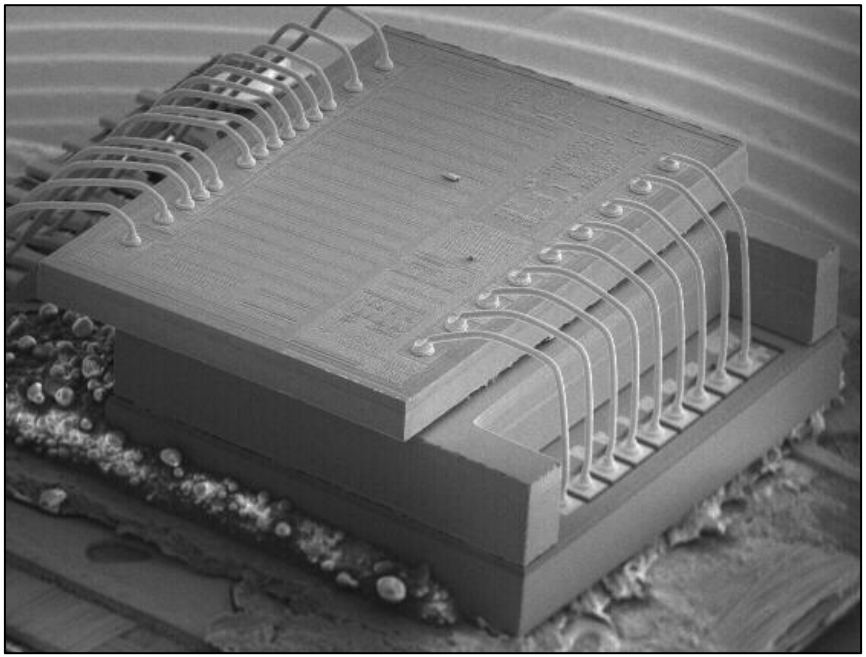
Reverse Costing analysis



STMicroelectronics LIS3DH / Apple A2L Triple-Axis MEMS Accelerometer

March 2011 - Version 1

Written by: Romain FRAUX

Table of Contents

- **LIS3DH Overview:**

Cristallo:

Ultra-Low-Power and High Performance Accelerometer

Higher flexibility at lower current

100X Lower Power

Courtesy of STMicroelectronics

Advanced power management

- Wide supply voltage down to 1.8V
- Ultra low current

High versatility

- Extended FS range (2/4/8/16g)
- Multiple configurable interrupt sources

Embedded features

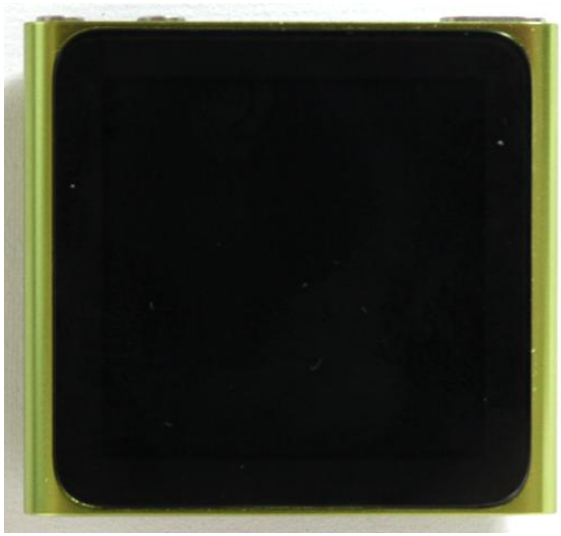
- Programmable FIFO (32 levels)
- 3 auxiliary ADC channels

Apple iPod Nano 6G Teardown

• **The LIS3DH is the official reference of the 3-Axis accelerometer integrated in the Apple iPod nano 6G, and labeled “A2L".**

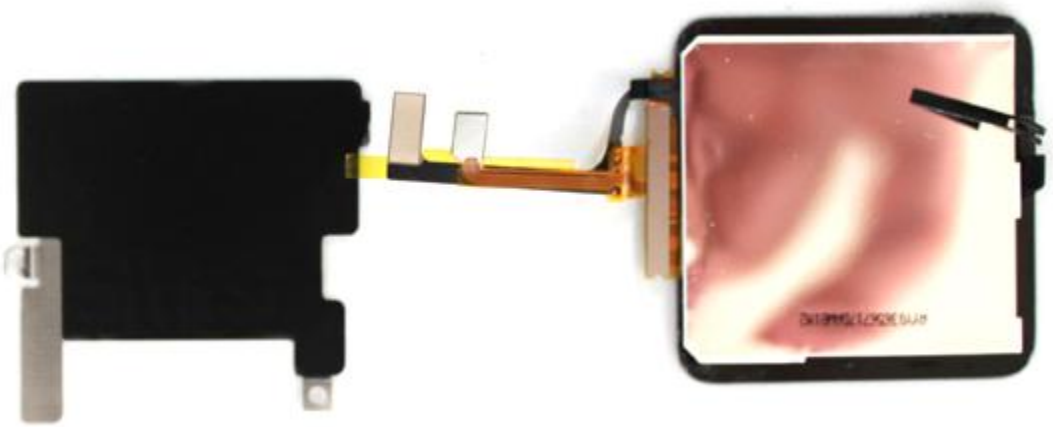
iPod nano 6G

Apple iPod Nano 6G Teardown



Front view

Back view

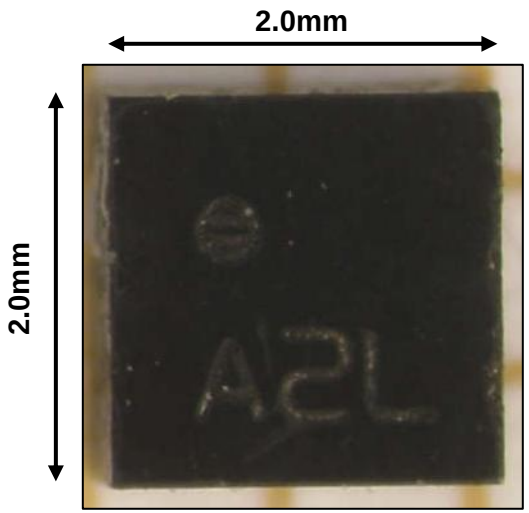


Display removed

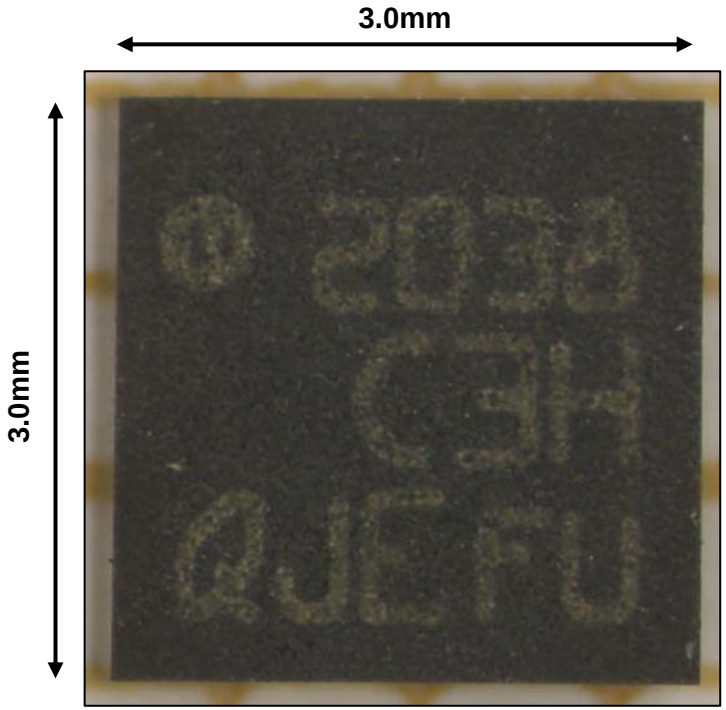
Packages Characteristics & Markings

Two references are analyzed:

- ✓ **STMicro LIS3DH: 3.0x3.0x1.0mm Package**
  - ➢ **STMicroelectronics standard component**
  - ➢ **Package Marking: C3H**
- ✓ **Apple A2L: 2.0x2.0x1.0mm Package**
  - ➢ **Apple iPod Nano 6G component**
  - ➢ **Package Marking: A2L**



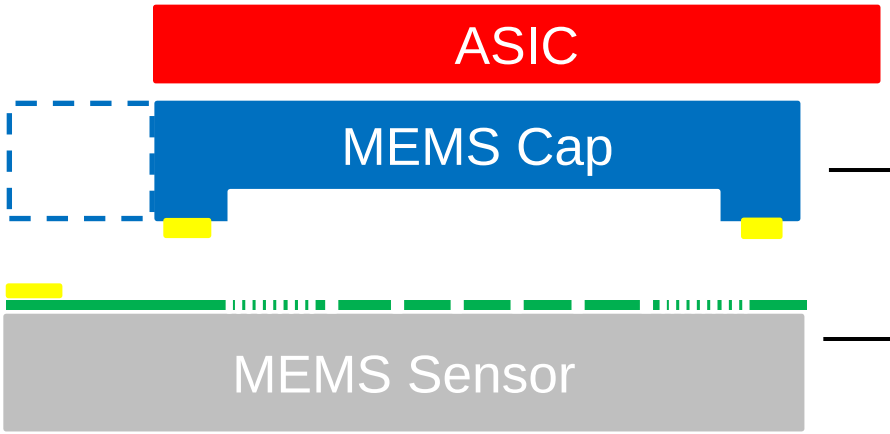
A2L



LIS3DH

Device Structure

The schematic diagram below is based on the observations made during this study and detailed in the next slides.



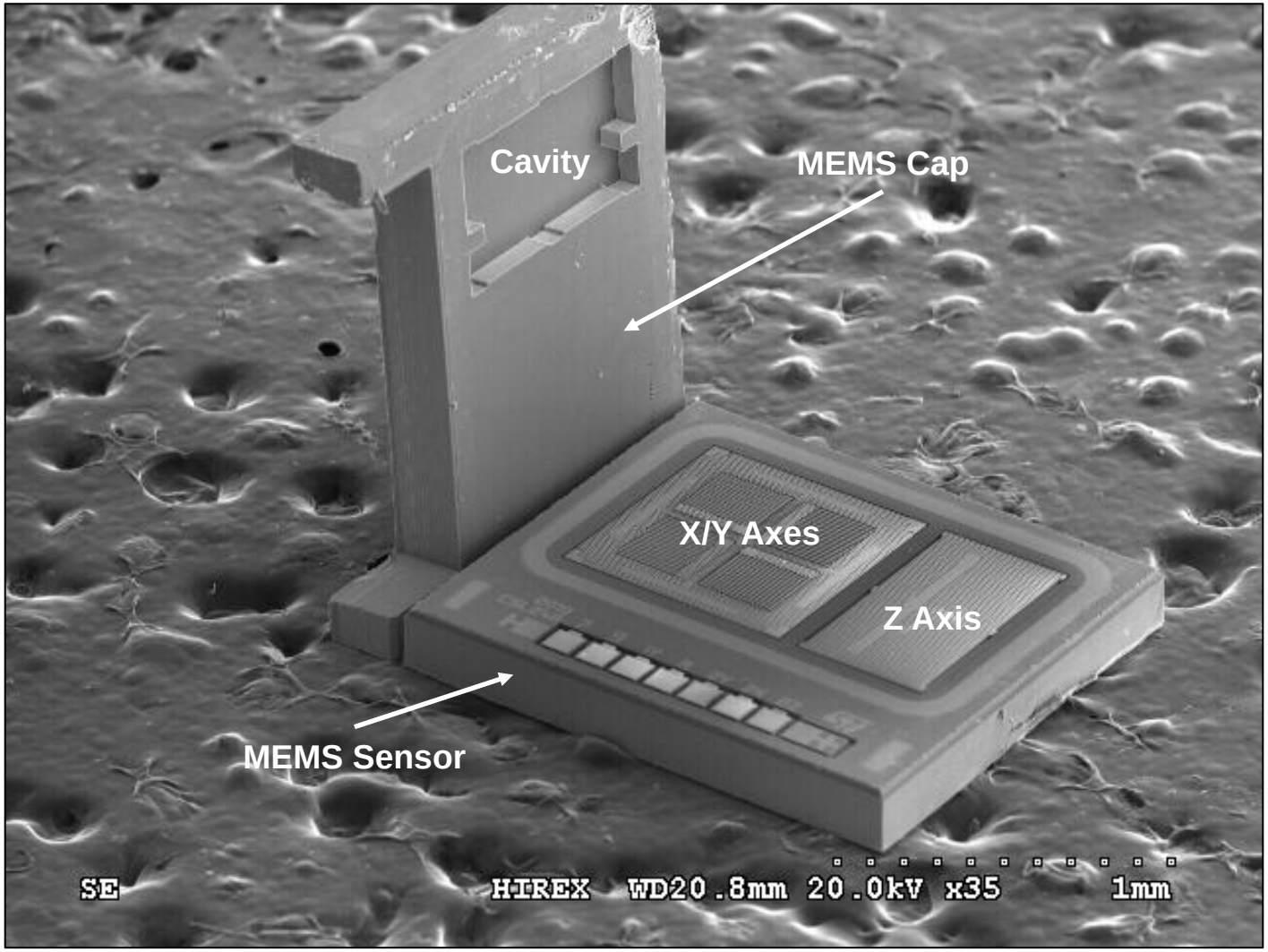
1. The **ASIC**
   - [illegible]
   - [illegible]

2. The **Cap**
   - [illegible]
   - [illegible]
   - [illegible]

3. The **Sensor**
   - [illegible]
   - [illegible]
   - [illegible]
   - [illegible]
   - [illegible]

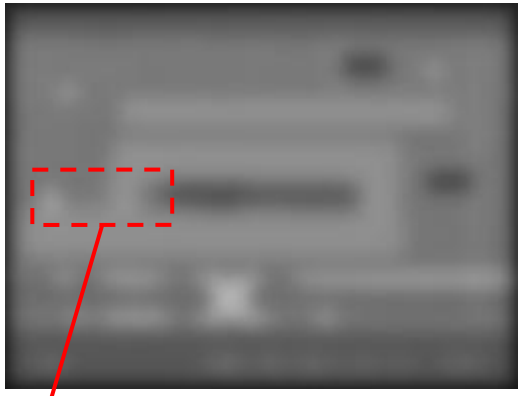
- [illegible]
- [illegible]
- [illegible]
- [illegible]

MEMS – Cap Opening

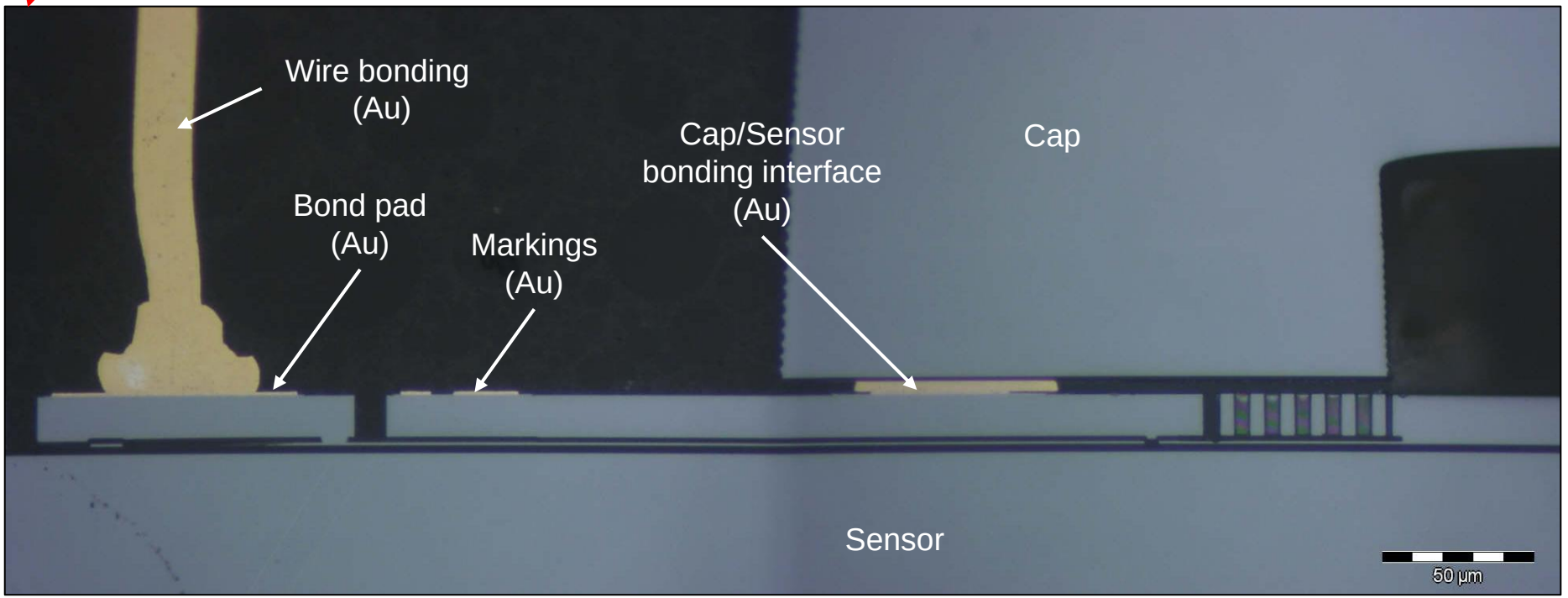


•**A cavity in the Cap is etched only above the Z-axis of the sensor.**

MEMS - Cross-Section



Cross-section Overview

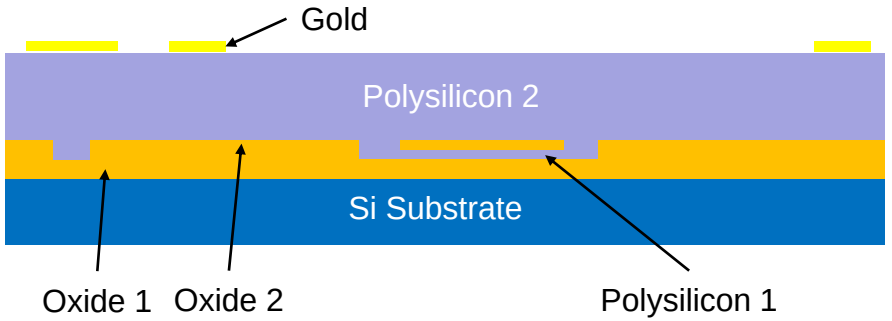


MEMS Cross-Section – Optical View

Sensor Process Flow

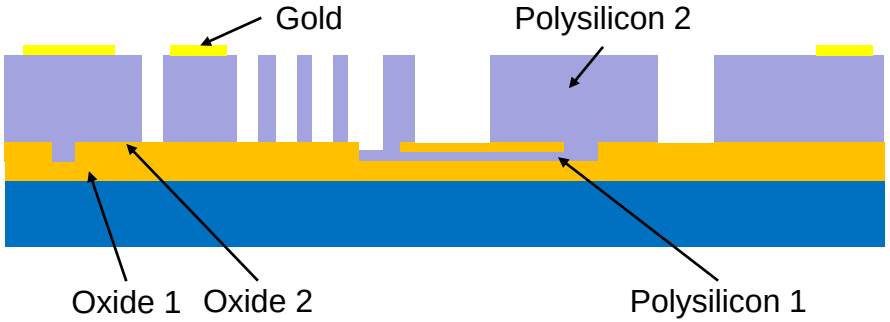
Sensor wafer

- Gold bond pads (lift-off patterning)



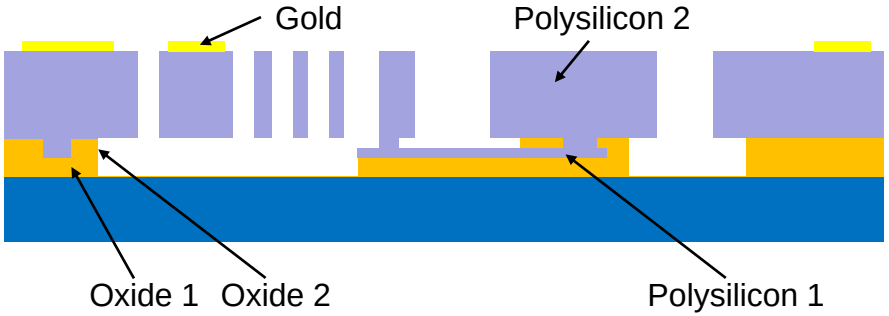
Sensor wafer

- Trench Etch (DRIE)

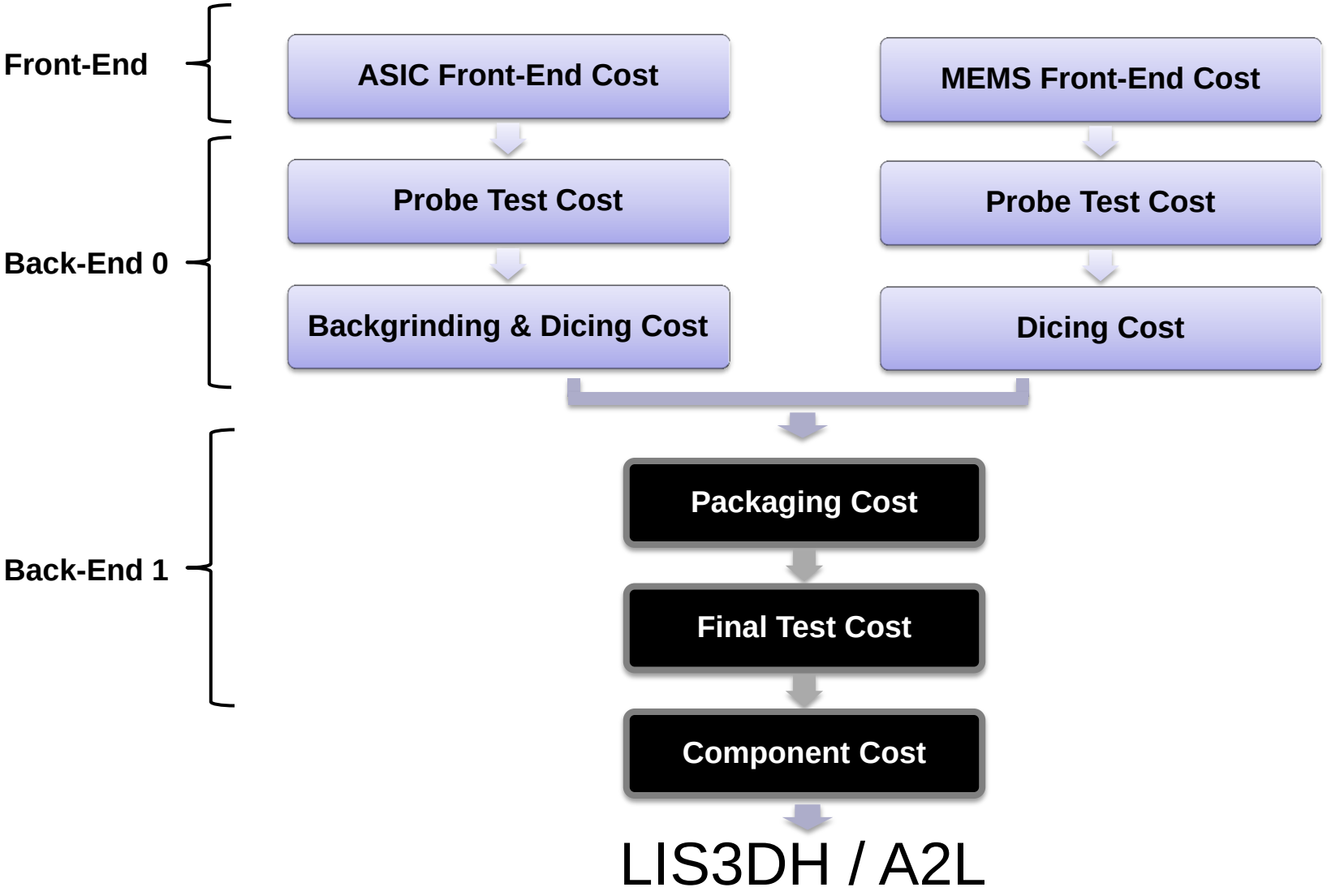


Sensor wafer

- Release (HF vapor etching)



Main steps of economic analysis



- We perform the economic analysis of the ASIC with the IC Price+ software.
- We perform the economic analysis of the MEMS and the packaging with the MEMS CoSim+ software.

ASIC Die Cost (Front-End + Back-End 0)

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Front-End Cost						
BE 0 : Probe Test						
BE 0 : Backgrinding						
BE 0 : Backgrinding yield losses						
BE 0 : Dicing Cost						
ASIC Wafer Cost						
Nb of potential dies per wafer						
Nb of good dies per wafer						
Front-End Cost						
BE 0 : Probe Test Cost						
BE 0 : Backgrinding Cost						
BE 0 : Dicing Cost						
BE 0 : Yield losses Cost						
ASIC Die Cost						

- **The ASIC die cost ranges from to according to yield variations.**
- **The main part of the ASIC die cost is due to with**
- **The back-end 0 yield ranges from to**

MEMS Front-End Cost

MEMS Front-End	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw Substrate Cost (2 x Si)						
Sensor Wafer						
Cap Wafer						
Bonding						
Yield losses						
MEMS Front-End Cost						

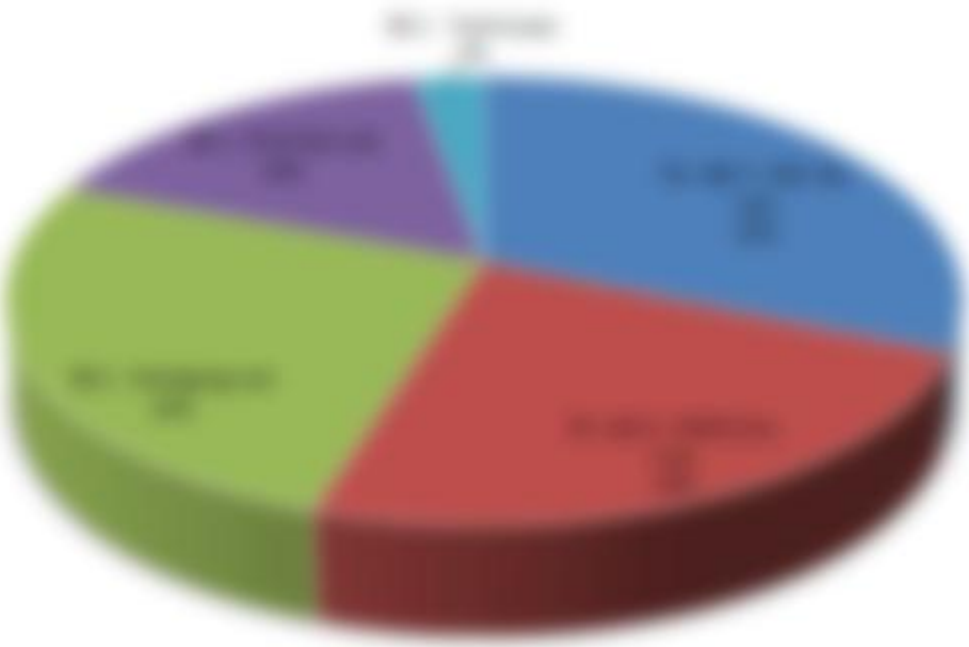
MEMS Manufacturing Cost Breakdown (Middle Yield)

- The [redacted] represents the main part of the manufacturing cost with [redacted]
- Due to the use of Gold for the wafer bonding, the cap wafer is more expensive than for the previous generations.

LIS3DH Component Cost (FE + BE 0 + BE 1)

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
FE + BE 0 : ASIC Die cost						
FE + BE 0 : MEMS Die Cost						
BE 1 : Packaging cost						
BE 1 : Final test cost						
BE 1 : Yield losses						
LIS3DH Component Cost						

LIS3DH Component Cost Breakdown (Medium Yields)



- **The component cost is between and according to yield variations.**
- **The die (ASIC + MEMS) represents of the total manufacturing cost.**
- **The packaging cost represents of the total manufacturing cost.**
- **Final test cost and yield losses (due to packaging and final test) represent of the total manufacturing cost.**