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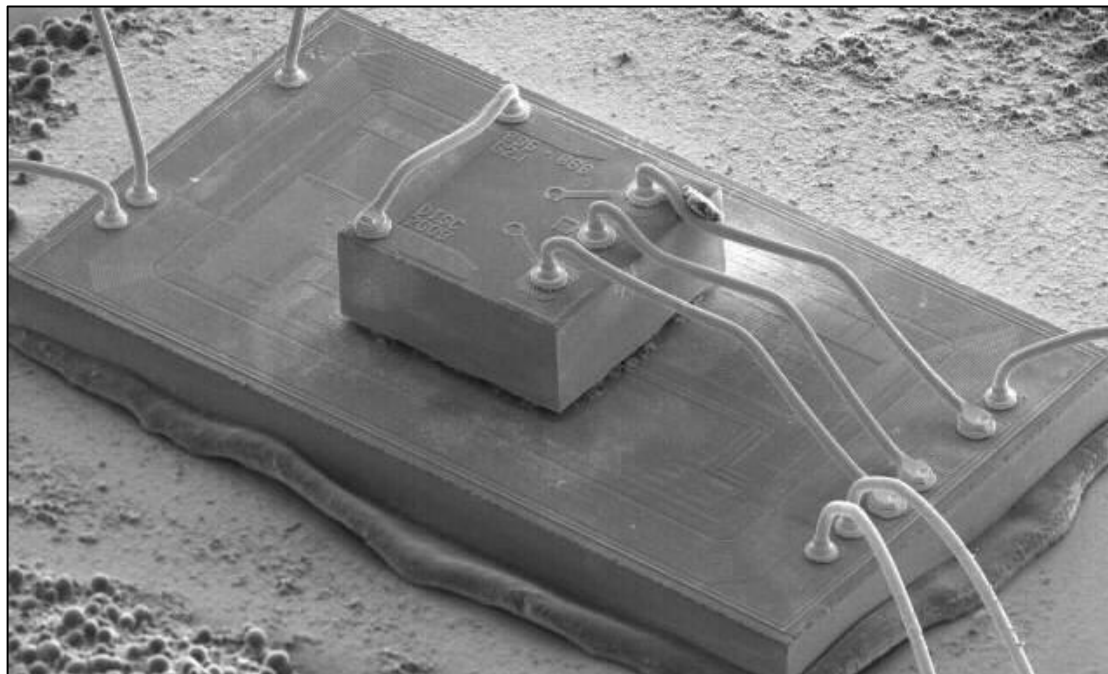
Reverse Costing analysis



Discera DSC8002 MEMS Oscillator

December 2010 - Version 1

Written by: Romain FRAUX

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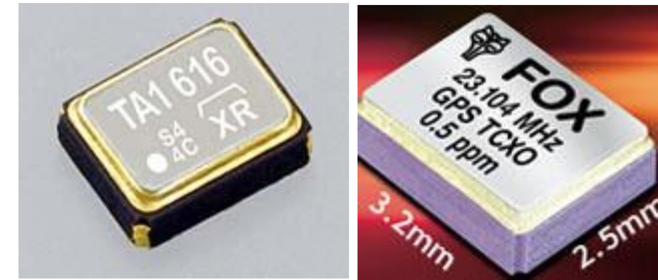
Overview of Oscillator Technologies

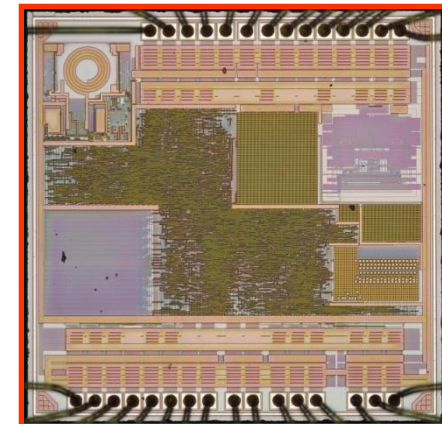
• Players & technologies (Courtesy of Yole Développement)

3 major technologies are competing in the timing market:

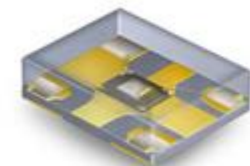
- **Quartz → the established technology**
  - **Many players: Epson, NDK, TXC, Kyocera, IDT, ICT, Fox Electronics, KDS, Rakon**
    - **Analog part of the oscillator is done by semiconductor companies: Cypress, Asahi, NPC…**
    - **Semiconductor IC players are integrating those quartz components into clock generators: IDT, Maxim, Silicon Labs, Cypress…**
- **CMOS → the low-end alternative**
  - **LC circuits (inductor-capacitor) can be used as resonators**
  - **Players Silicon Labs, Mobius microsystems (acquired by IDT in Jan. 2010), Linear Technology, Cypress…**
- **MEMS → the disruptive technology**
  - **Players: SiTime, Discera, Silicon Clocks**
    - **In dev: Sand9, NXP, TXC, CSEM (with AIN piezo layer similar principle to the quartz principle)**
- **Alternative technologies (niche markets): rubidom atomic oscillator, cesium…**



Epson Toyocom / Fox Electronics oscillators



Integration of Mobius Microsystems CMOS oscillator



Ecliptek EMO MEMS oscillator

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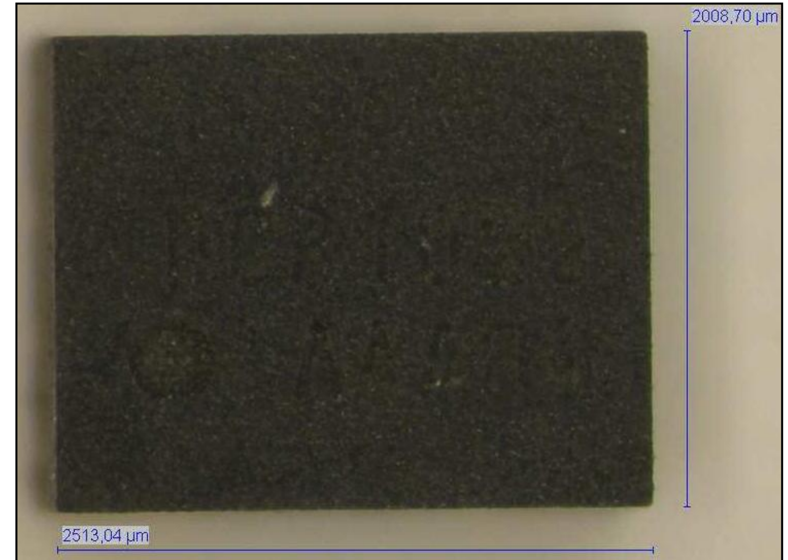
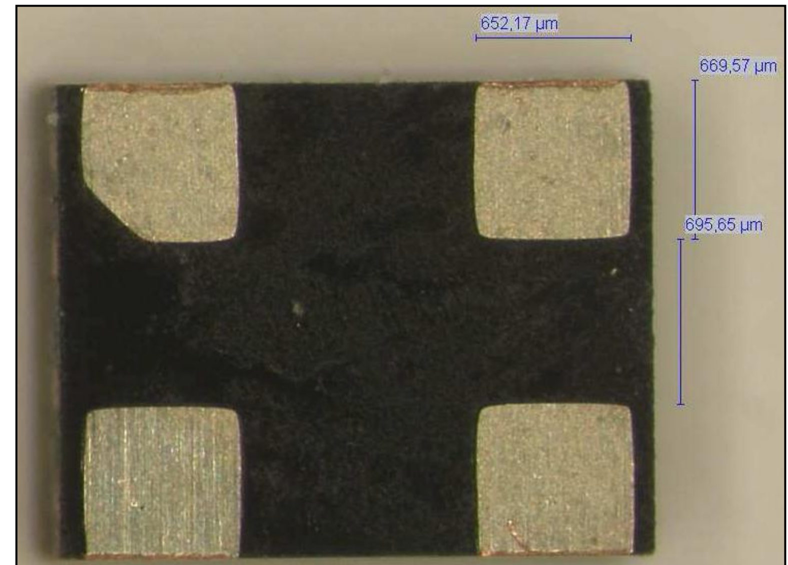
DSC8002D

- **Package type:** 4-pin MLF
- **Dimensions:** 2.5mm x 2.0mm x 0.85mm
- **Marking:** DCP1029
  AAAOQ



Package Top view

Package Marking



Package Back view

Package Side view

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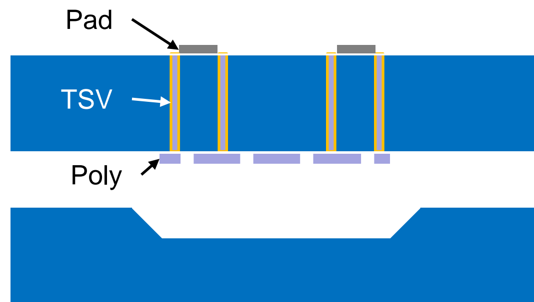
Device Structure

The schematic diagram below is based on the observations made during this study and detailed in the next slides.



1. The **Resonator**

- Connections via (TSV) etched by DRIE

2. The **Cap**

- Bulk micromachining

3. The **ASIC**

- CMOS 0.18µm 6M 1P

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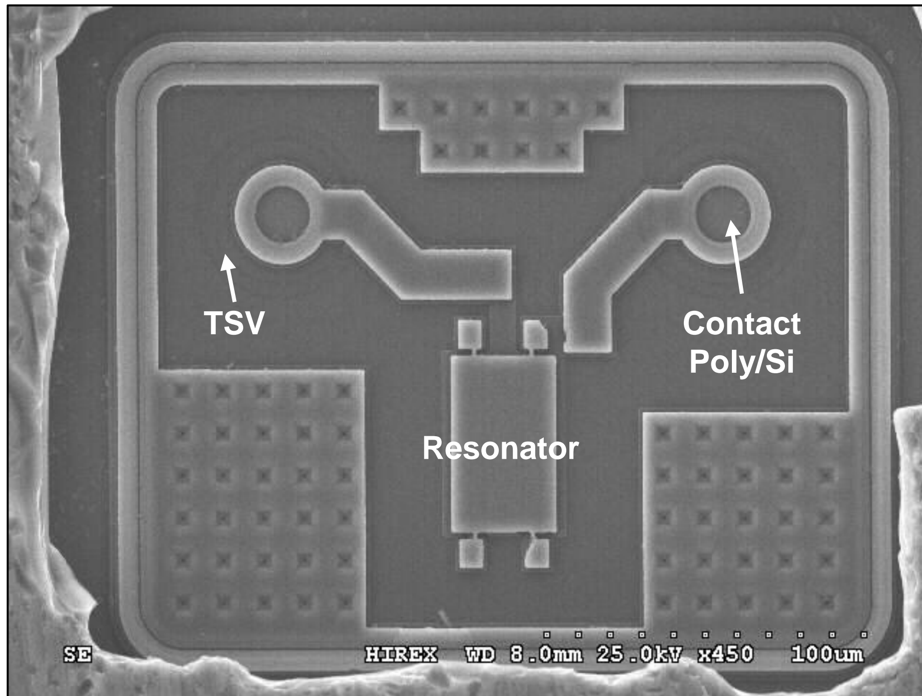
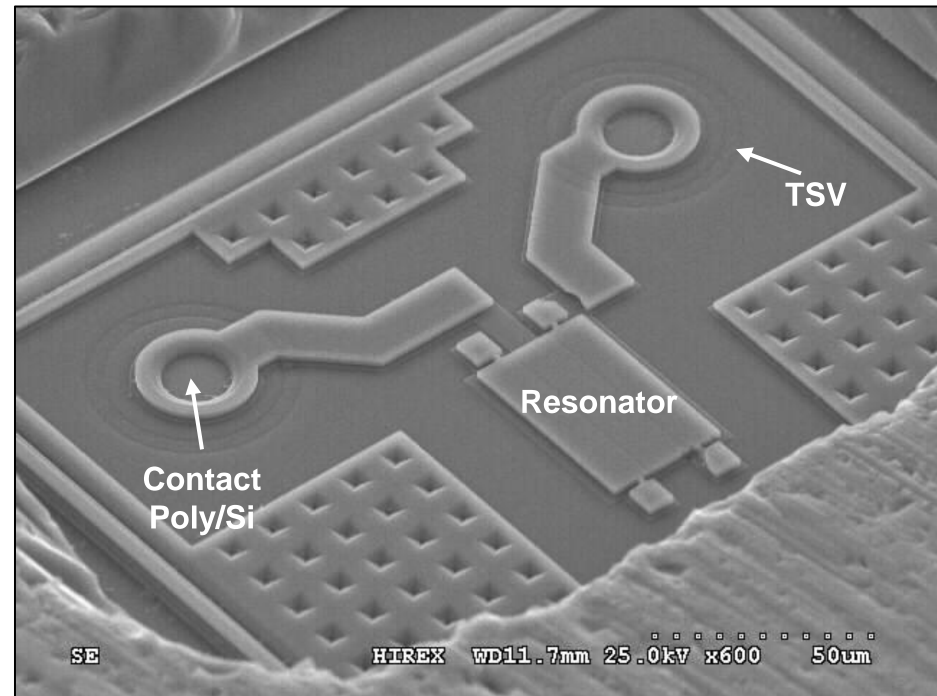
MEMS – Resonator



Resonator with connections – SEM View



Resonator with connections – Tilted SEM View

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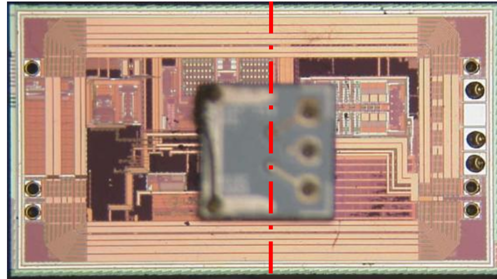
MEMS - TSV Cross-Section



Cross-Sectional Plane BB'

Resonator

TSV

Cap

ASIC

100 µm

AA' Cross Section Overview

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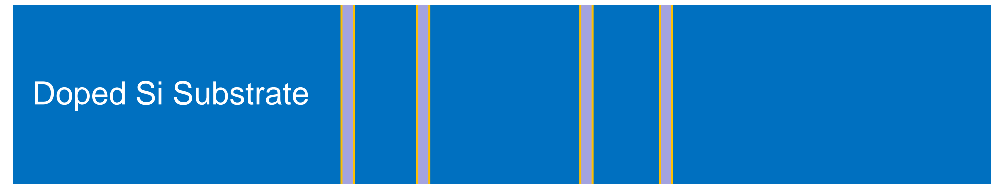
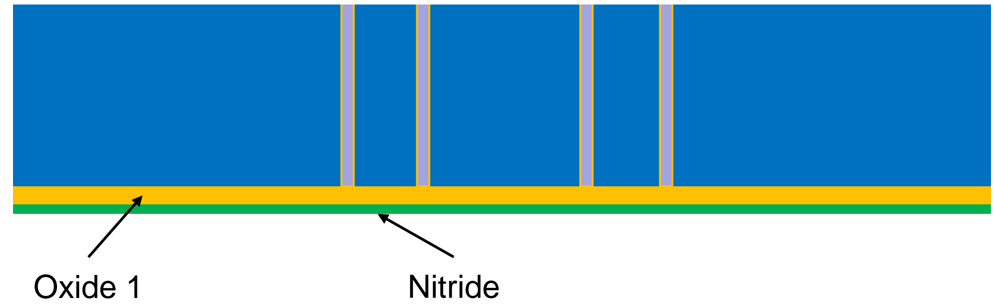
MEMS Process Flow – Resonator

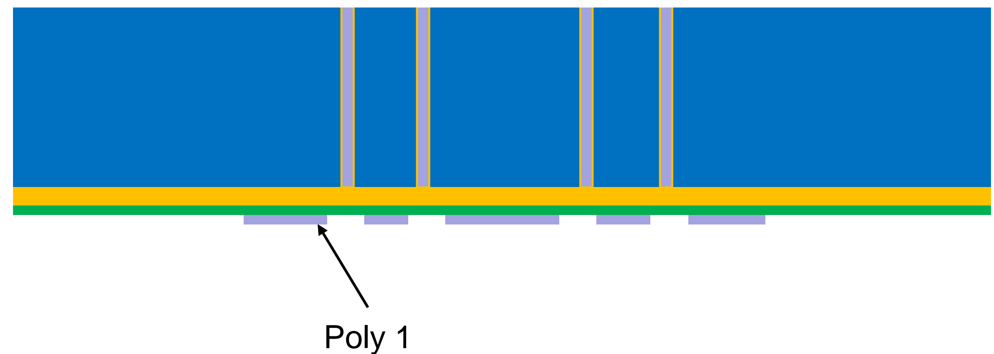
- Substrate with TSV



- Isolation (SiO_2+SiN)



- Polysilicon 1 (Deposition + Pattern)



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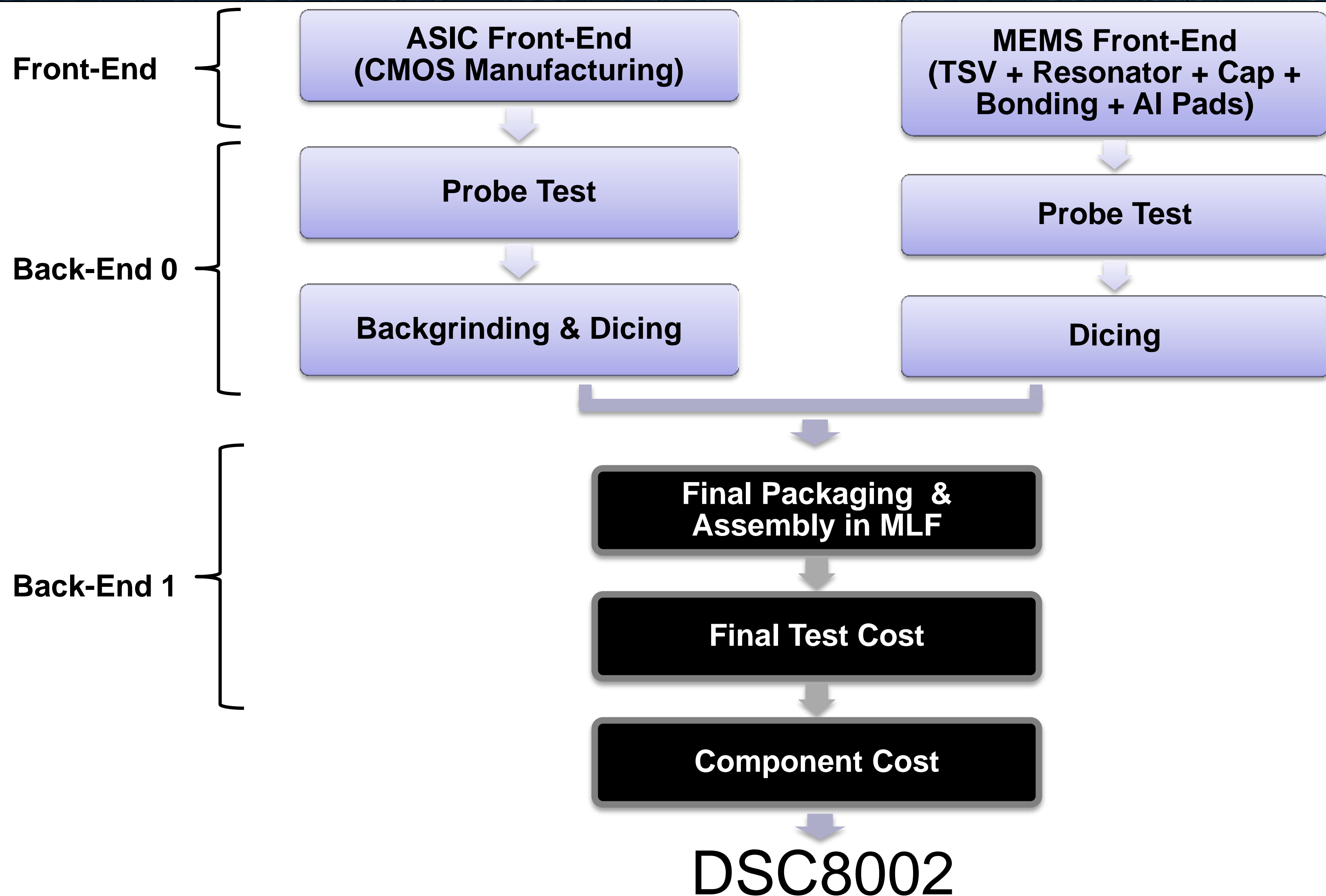
Main steps of economic analysis



- We perform the economic analysis of the ASIC with the IC Price+ software.
- We perform the economic analysis of the MEMS and the packaging with the MEMS CoSim+ software.

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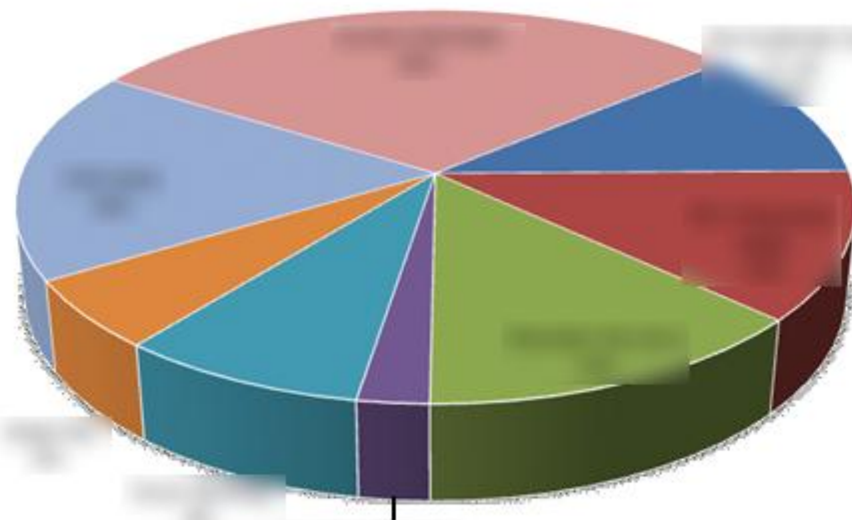
MEMS Front-End Cost

MEMS Front-End	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw Substrate Cost (2 x Si)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
TSV in Resonator Wafer	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Resonator Structure	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Cap Manufacturing	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Fusion Bonding	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Metal Pad	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MEMS Front-End Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Foundry Overhead	[illegible]		[illegible]		[illegible]	
MEMS Unprobed Wafer Cost	[illegible]		[illegible]		[illegible]	

MEMS Unprobed Wafer Cost Breakdown (Middle Yield)



- **The manufacturing of the [illegible] represents the main part of the front-end manufacturing cost with [illegible]**

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MEMS FE Cost per Process Steps (2/3)

Resonator Wafer	Cost	Breakdown
Isolation - Cleaning	[illegible]	[illegible]
Isolation - Oxide 1 Deposition [illegible]	[illegible]	[illegible]
Isolation - Measurement	[illegible]	[illegible]
Isolation - SiN Deposition [illegible]	[illegible]	[illegible]
Isolation - Measurement	[illegible]	[illegible]
Poly 1 - Cleaning	[illegible]	[illegible]
Poly 1 - Polysilicon Deposition [illegible]	[illegible]	[illegible]
Poly 1 - Measurement	[illegible]	[illegible]
Poly 1 - Doping	[illegible]	[illegible]
Poly 1 - Cleaning	[illegible]	[illegible]
Poly 1 - Pattern 2	[illegible]	[illegible]
Poly 1 - Etching Poly 1	[illegible]	[illegible]
Poly 1 - PR Removal	[illegible]	[illegible]
TOTAL	[illegible]	[illegible]

Resonator Manufacturing Step Cost Breakdown

Isolation - Cleaning
Isolation - Oxide 1 Deposition
Isolation - Measurement
Isolation - SiN Deposition
Isolation - Measurement
Poly 1 - Cleaning
Poly 1 - Polysilicon Deposition
Poly 1 - Measurement
Poly 1 - Doping
Poly 1 - Cleaning
Poly 1 - Pattern 2
Poly 1 - Etching Poly 1
Poly 1 - PR Removal

Resonator Manufacturing Steps Cost (Simulated with MEMS CoSim+ Cost Simulation Tool)

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MEMS Die Cost (Front-End + Back-End 0)

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Front-End Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Probe Test Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Dicing Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MEMS Wafer Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Nb of potential dies per wafer	[illegible]		[illegible]		[illegible]	
Nb of good dies per wafer	[illegible]		[illegible]		[illegible]	
Front-End Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Probe Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Dicing Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MEMS Die Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

- **The MEMS die cost ranges from [illegible] according to yield variations.**
- **The Front-end cost (raw Si substrates, wafer processing and yield losses) represents around [illegible] of the die cost.**
- **The Back-End 0 cost (Probe test, dicing and yield losses) represents [illegible] of the die cost.**

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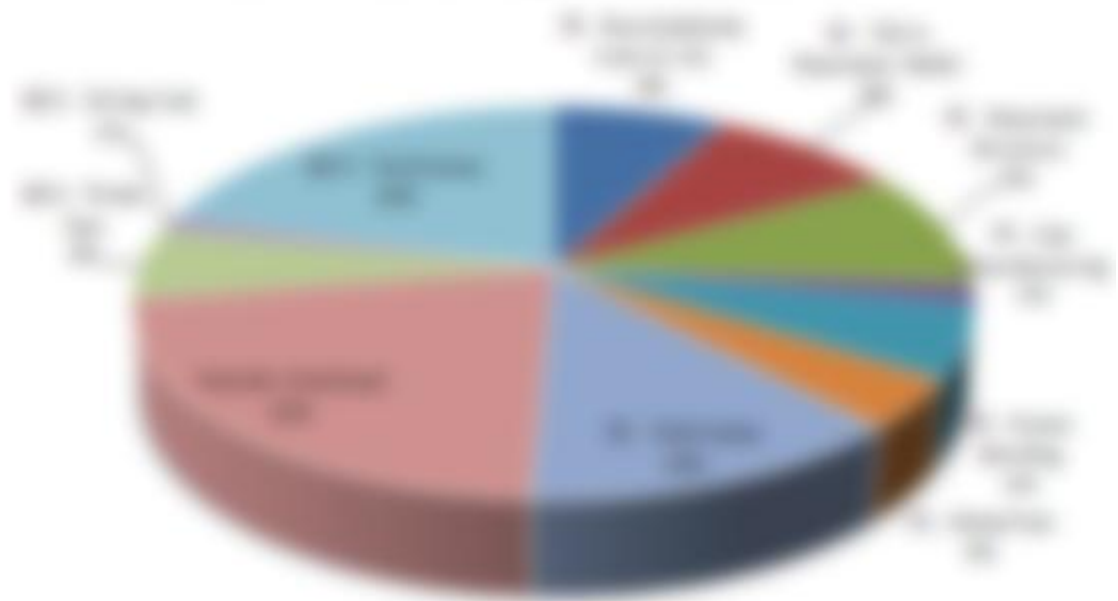
MEMS Die Cost (Front-End + Back-End 0)

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
FE : Raw Substrate Cost (2 x Si)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : TSV in Resonator Wafer	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Resonator Structure	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Cap Manufacturing	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Fusion Bonding	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Metal Pad	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Foundry Overhead	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Probe Test	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Dicing Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MEMS Die Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

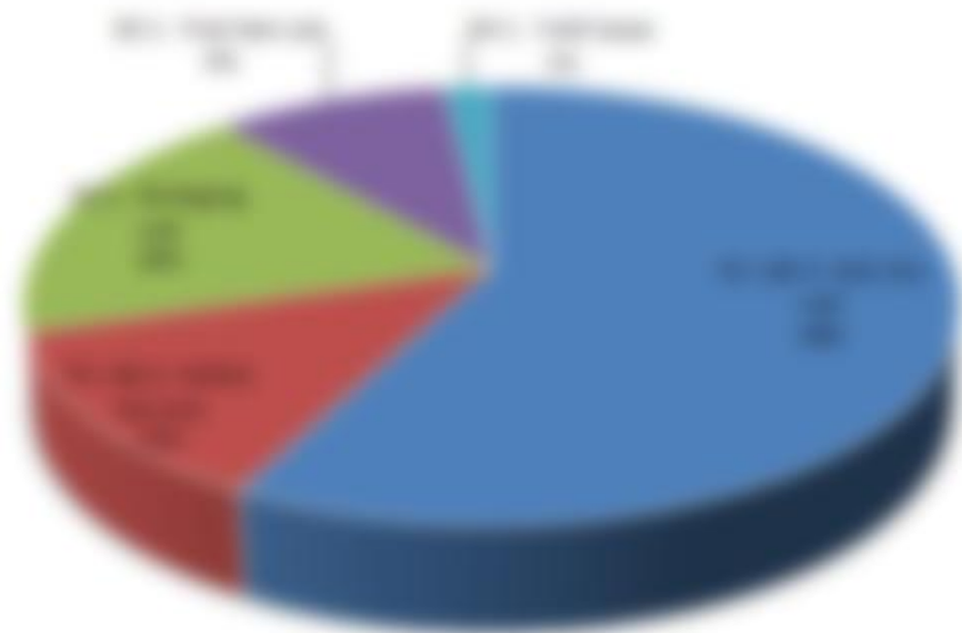
MEMS Die Cost Breakdown (Medium Yield)



DSC8002 Component Cost (FE + BE 0 + BE 1)

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
FE + BE 0 : ASIC Die cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE + BE 0 : MEMS Die Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 1 : Packaging cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 1 : Final test cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 1 : Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
DSC8002 Component Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

DSC8002 Component Cost Breakdown (Medium Yields)



- **The component cost is between [illegible] [illegible] according to yield variations.**
- **The die (ASIC + MEMS) represents [illegible] of the total manufacturing cost.**
- **The packaging cost represents [illegible] of the total manufacturing cost.**
- **Final test cost and yield losses (due to packaging and final test) represent [illegible] of the total manufacturing cost.**

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