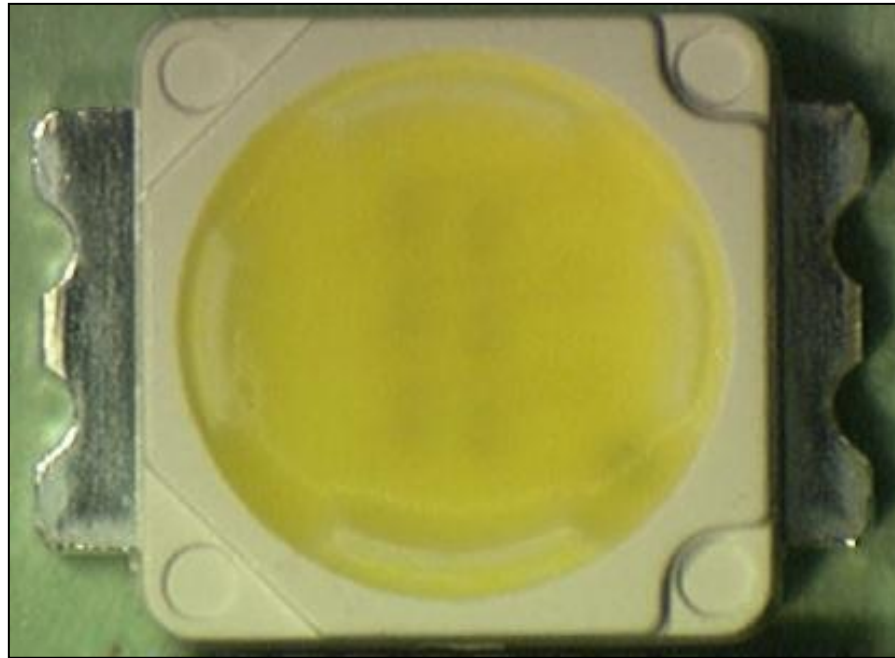


Reverse Costing analysis



Nichia NS6W183T

August 2010 - Version 2

Written by: Sylvain HALLEREAU

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Version 2 : We have add one slide on the active layers thicknesses (slide 28). The new picture give more precise measures of MQW and p-GaN layers thicknesses. With the new data, we have re-calculate the epitaxy step cost (slide 51).

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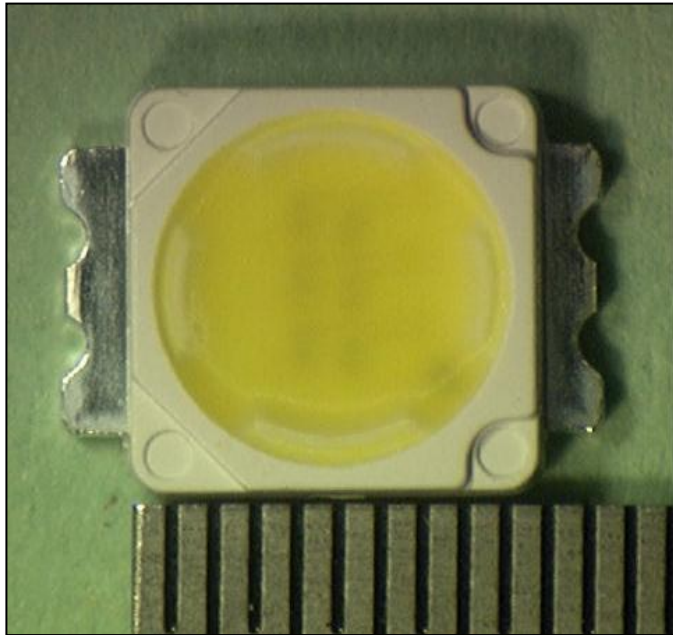
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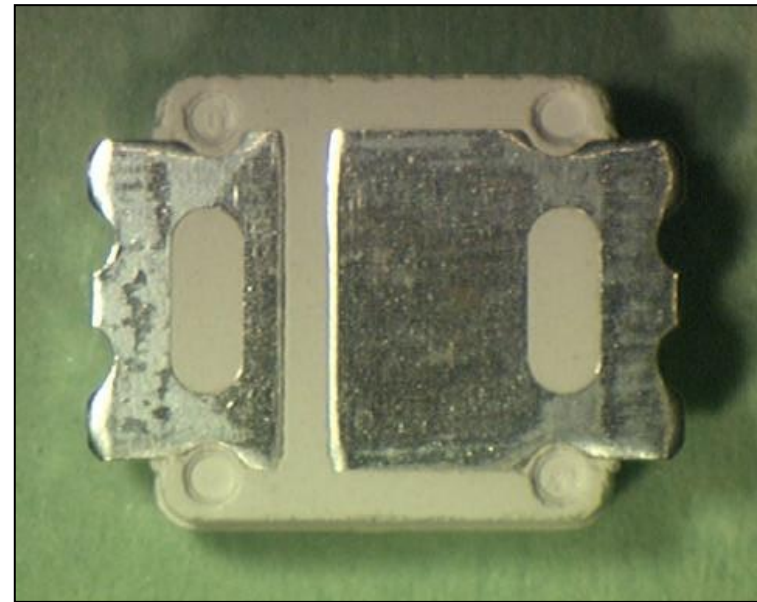
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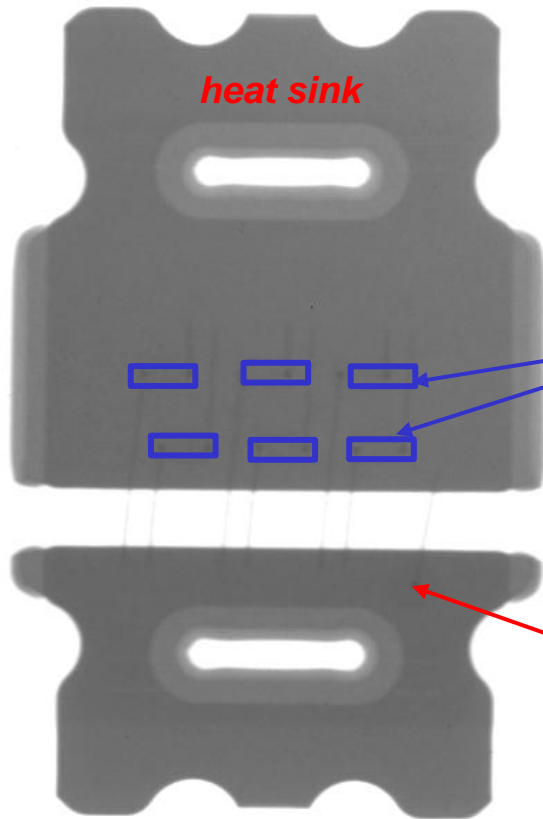
Top view of the NS6W183T. The NS6W183T package is 6.5 x 4.3mm in dimension.



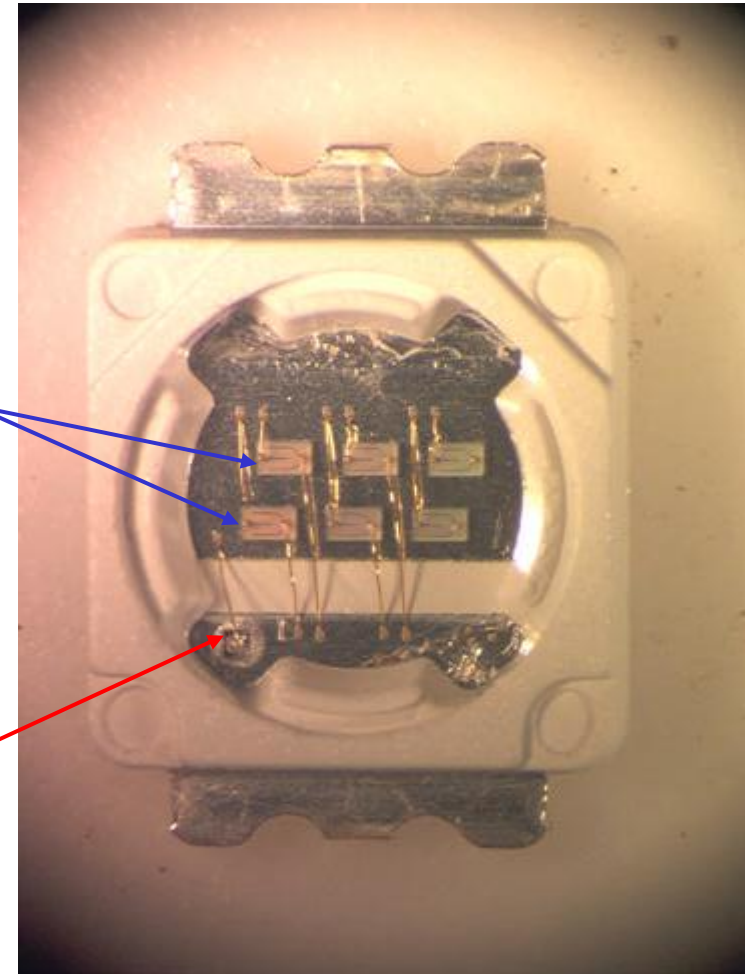
Underside view of the NS6W183T.



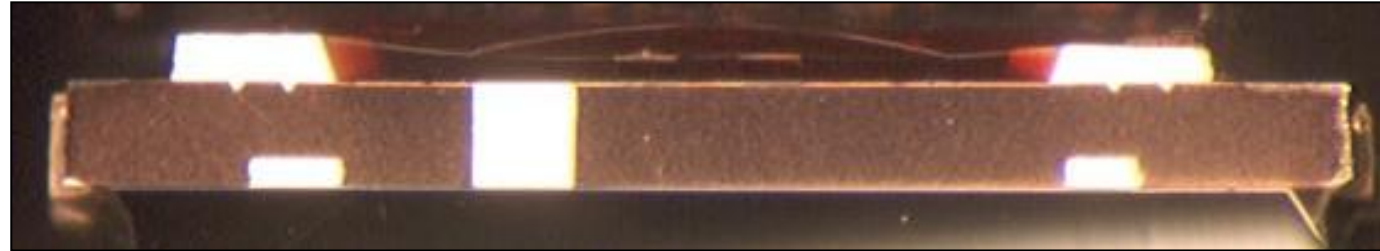
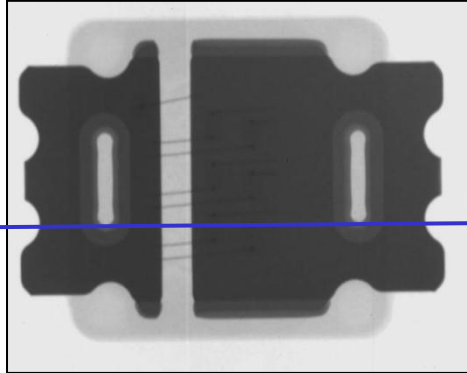
Edge view of the NS6W183T



Plan view XRAY image shows the lead frame configuration.



Top view with fluorescent medium removed

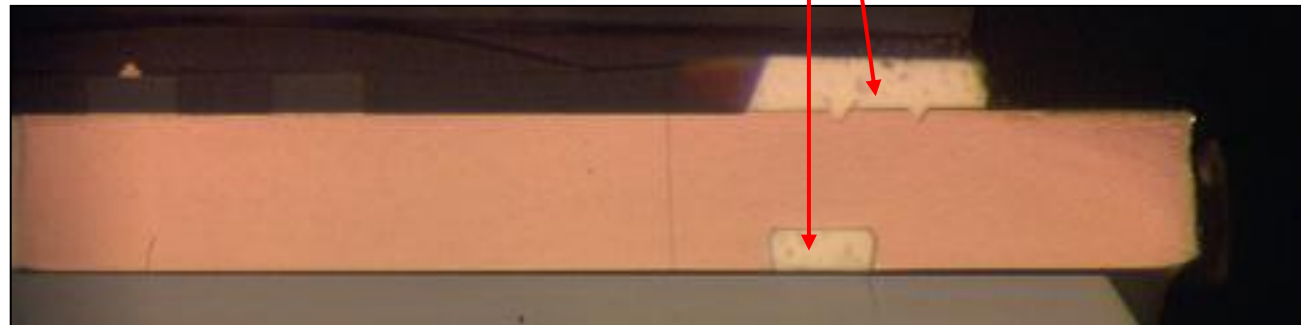


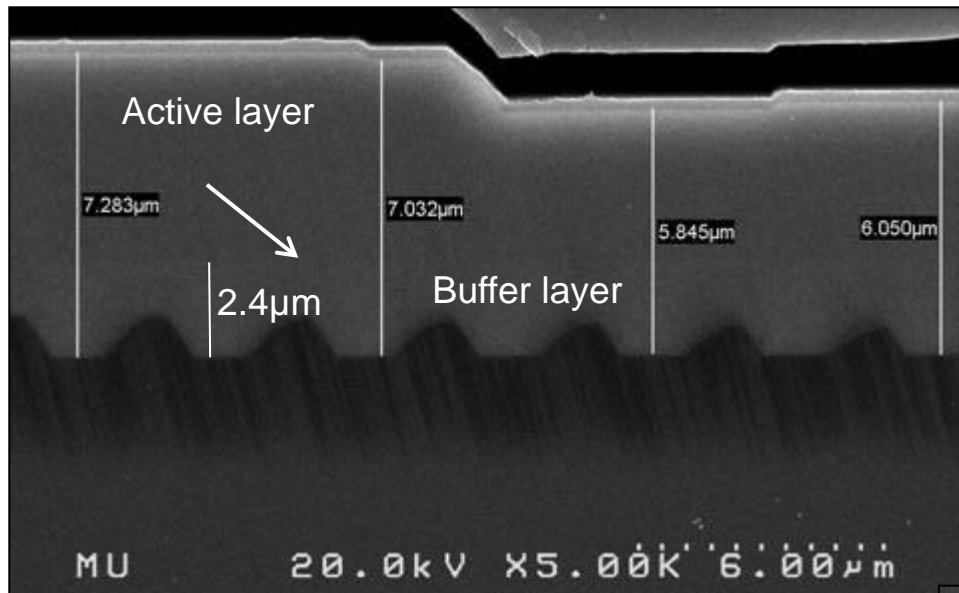
Package cross-section, roughly at the line in the XRAY above.



Higher magnification images of the cross-section.

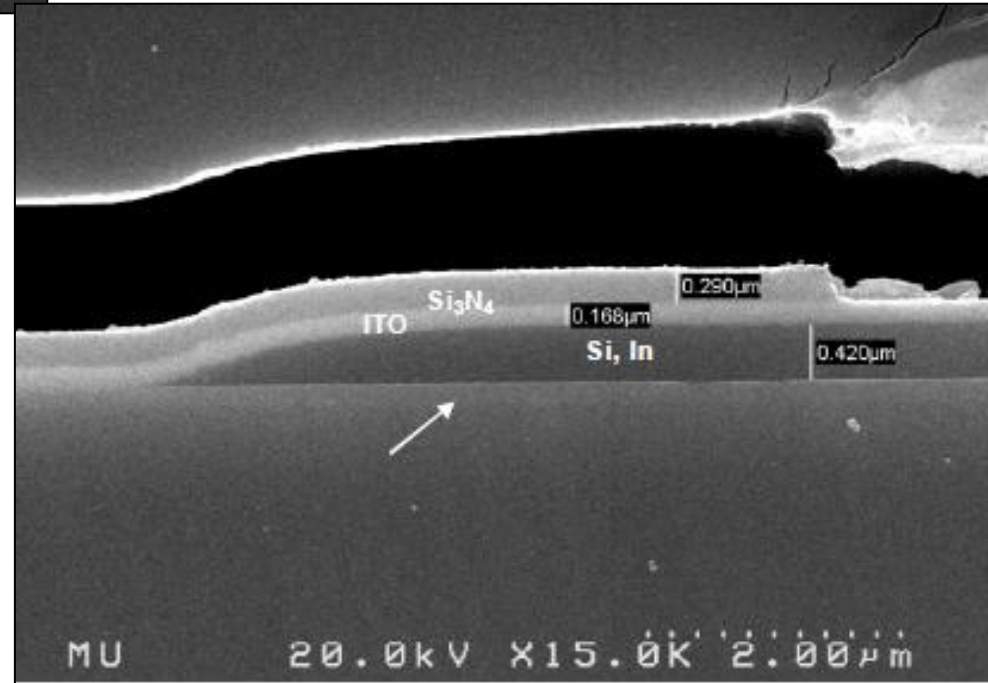
Epoxy molded around two metal electrodes acting as heat sink

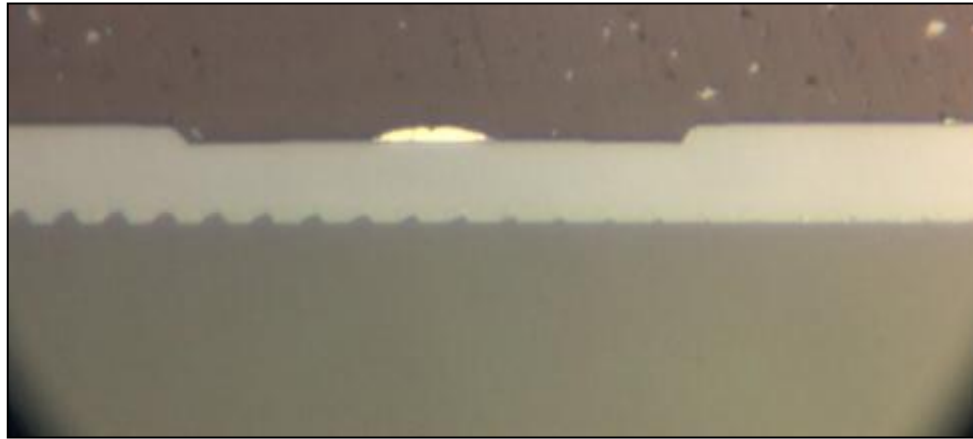




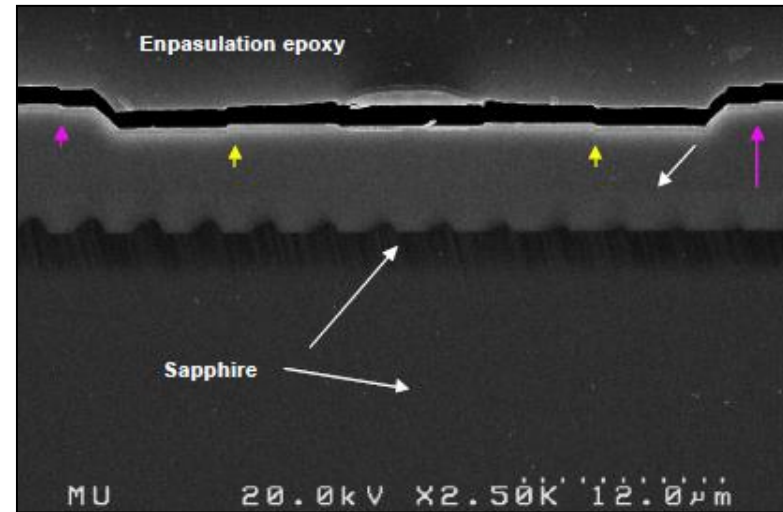
SEM view : Thickness of the active GaN Layer. The white arrow points to border between the buffer layer (2.4 μm) and the active layer.

SEM view : The white arrow points to a faint line in the GaN substrate, the MQW.



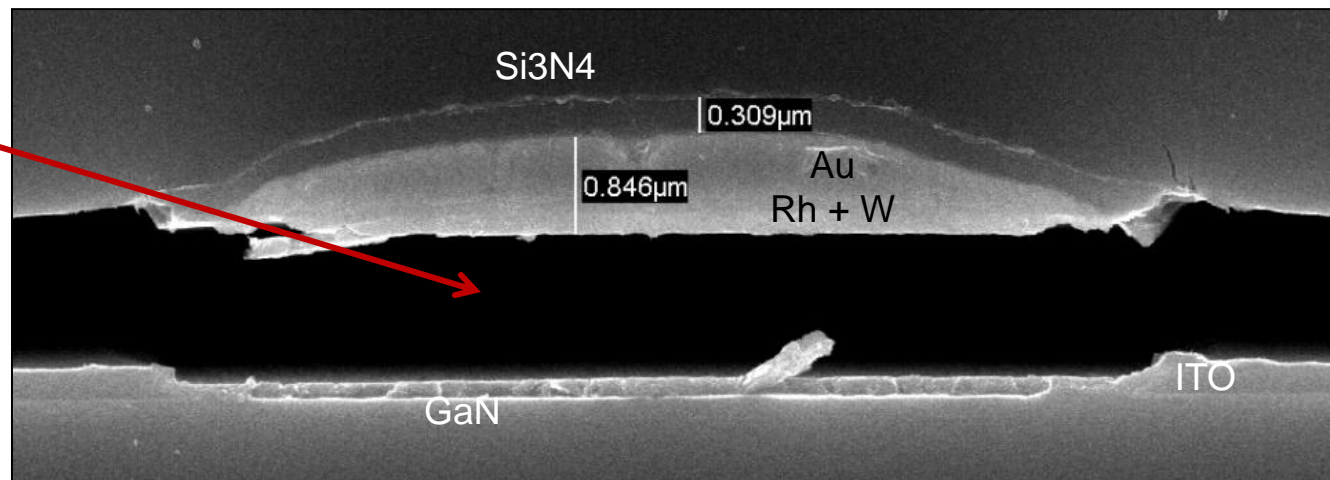


Optical image : the cathode



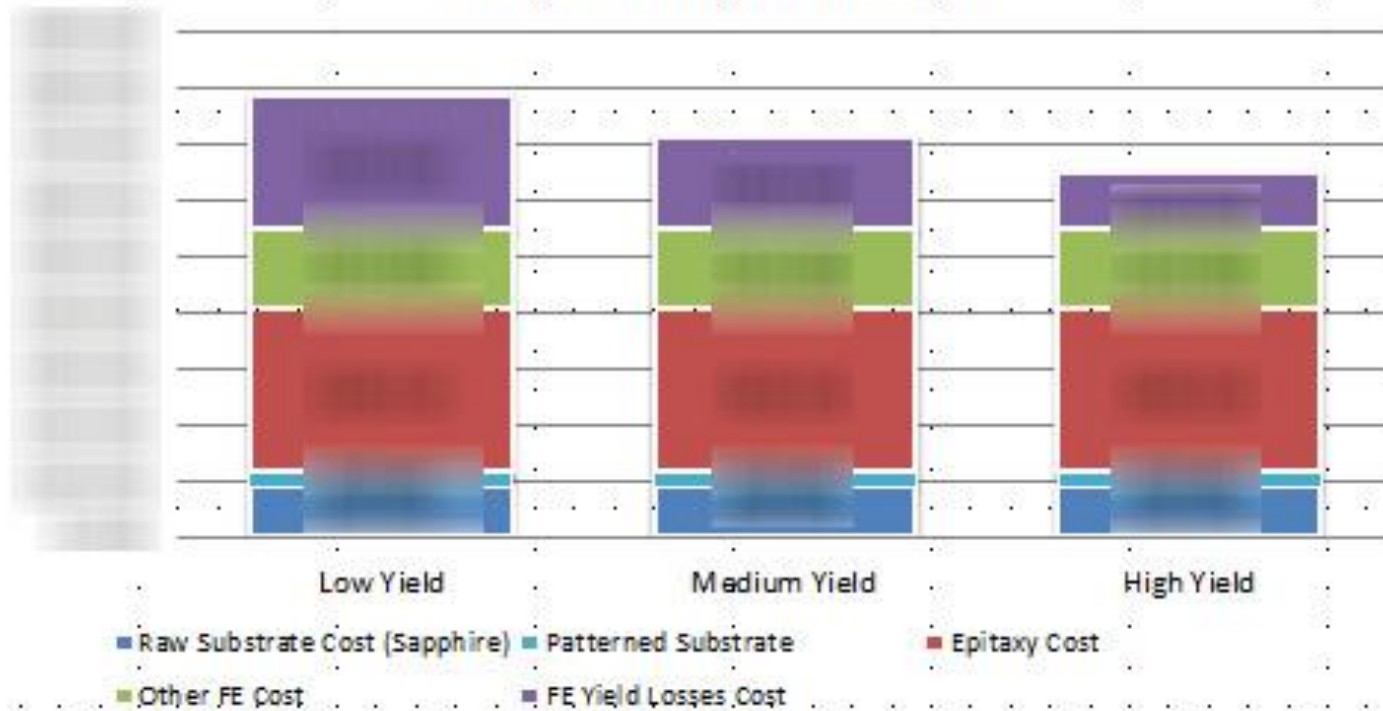
The polishing has caused the gold trace to lift.

Cathode trace in gold. It sits directly on ITO. A thin W-Rh adhesion layers for the gold traces is deposited.



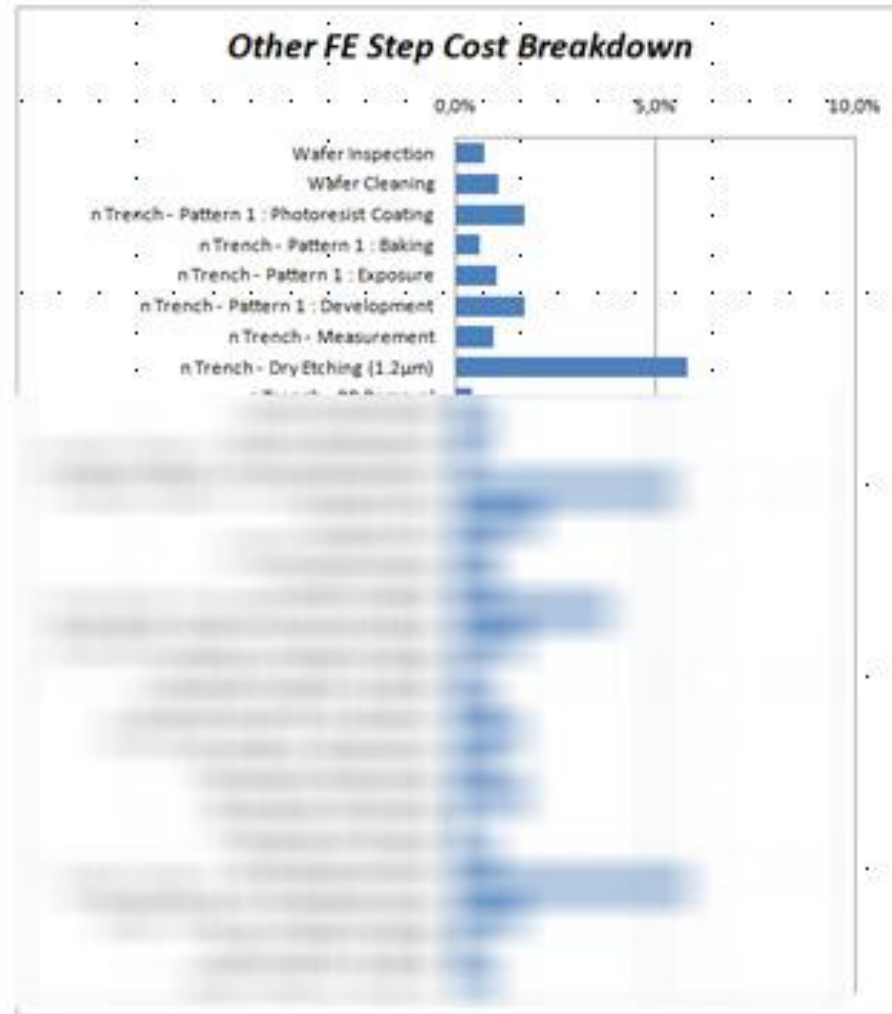
| Total Front-End | Low Yield | | Medium Yield | | High Yield | |
|-------------------------------|-----------|------------|--------------|------------|------------|------------|
| | Cost | Break down | Cost | Break down | Cost | Break down |
| Raw Substrate Cost (Sapphire) | | | | | | |
| Patterned Substrate | | | | | | |
| Epitaxy Cost | | | | | | |
| Other FE Cost | | | | | | |
| FE Yield Losses Cost | | | | | | |
| TOTAL Front-End Cost | | | | | | |

Front-End Cost Breakdown



•Details of the equipment cost per step are given in the Excel Spreadsheet.

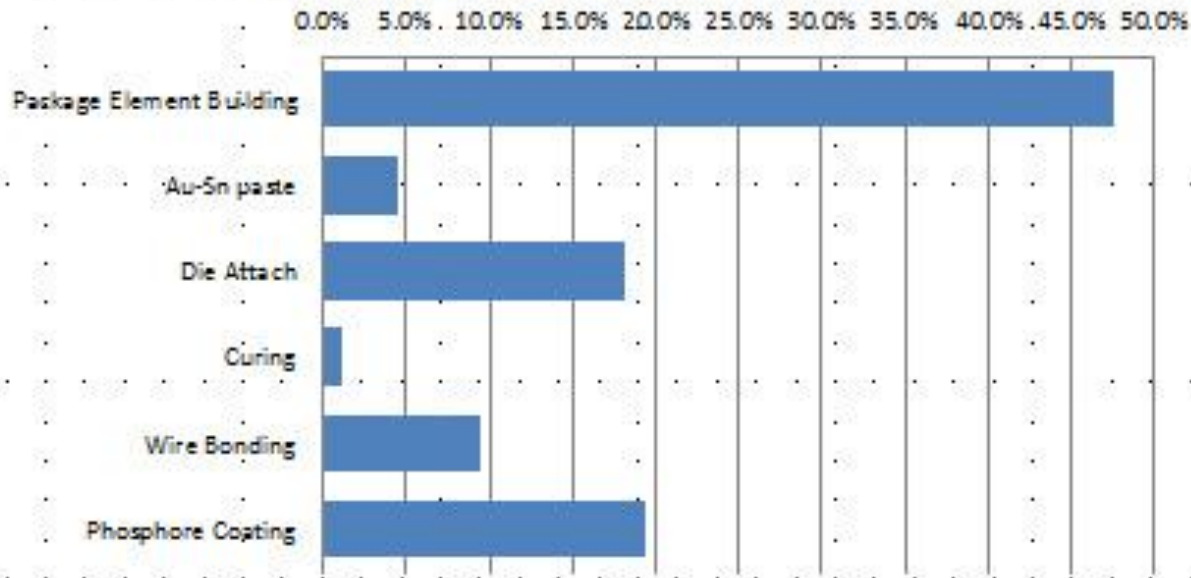
| Other FE Steps | Cost | Breakdown |
|--|------|-----------|
| Wafer Inspection | | |
| Wafer Cleaning | | |
| n Trench - Pattern 1 : Photoresist Coating | | |
| n Trench - Pattern 1 : Baking | | |
| n Trench - Pattern 1 : Exposure | | |
| n Trench - Pattern 1 : Development | | |
| n Trench - Measurement | | |
| n Trench - Dry Etching (1.2µm) | | |
| n Trench - PR Removal | | |
| n Trench - Measurement | | |



| Packaging Process Step | Cost | Breakdown |
|--------------------------|------|-----------|
| Package Element Building | | |
| Au-Sn paste | | |
| Die Attach | | |
| Curing | | |
| Wire Bonding | | |
| Phosphore Coating | | |
| TOTAL | | |

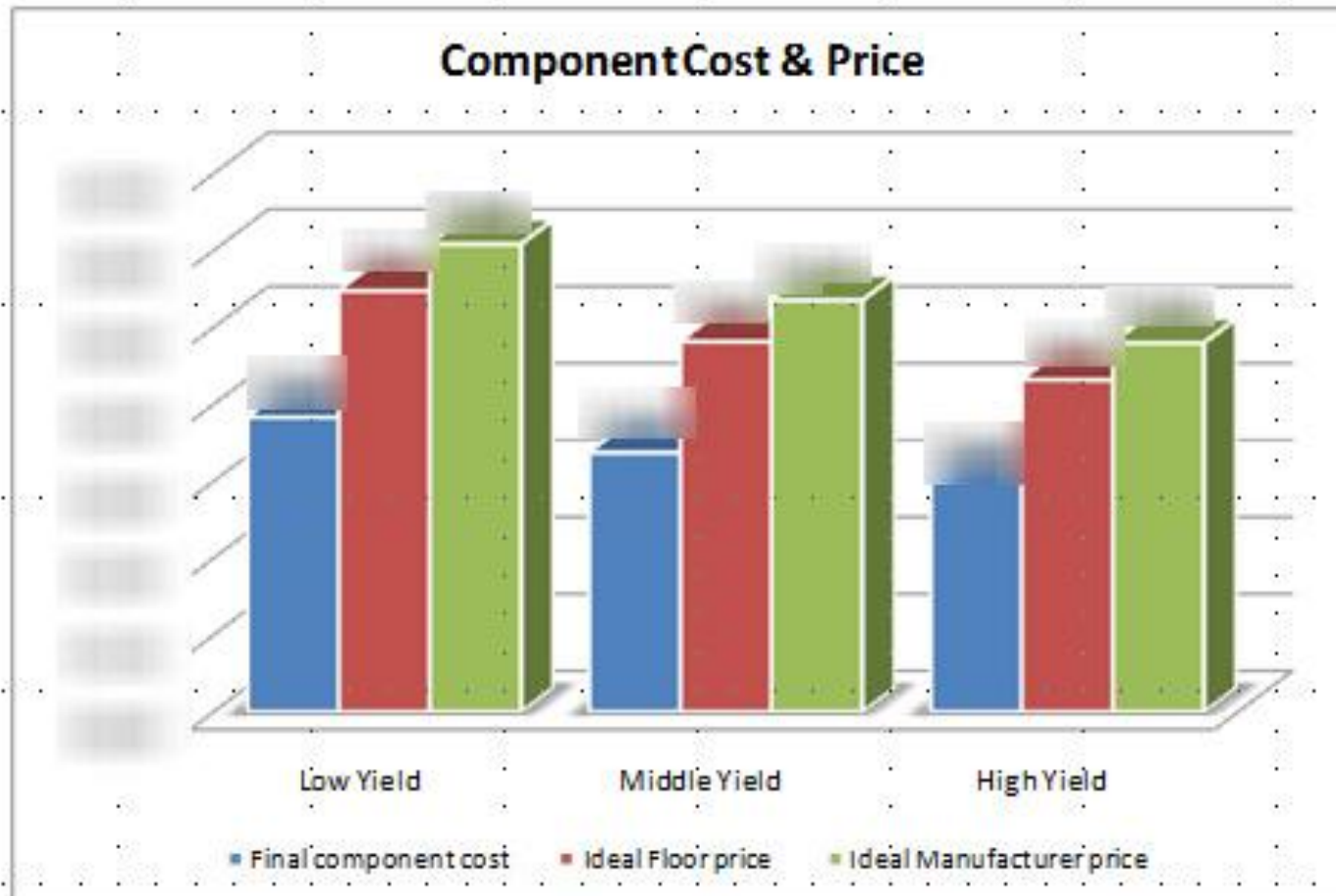
- The total packaging cost is estimated to [REDACTED]
- The cost by step includes the equipment cost, the material cost and the labour cost.

Packaging Step Cost Breakdown



| Versions | Final component cost | Ideal Floor price | Ideal Manufacturer price |
|--------------|----------------------|-------------------|--------------------------|
| Low Yield | | | |
| Middle Yield | | | |
| High Yield | | | |

The ideal manufacturer price is obtained for a binning yield of 100%.



Advantages :

- The probe yield is better.
- 6 LEDs could be selected to get the right brightness, color. The final binning can be improved.

Inconvenients :

- The multiple LEDs solution increases the probe test and dicing cost.

• Reverse costing analysis represents the best cost/price evaluation given the publically available data, completed with industry expert estimates.

- These results are open for discussion. We can re-evaluate this circuit with your information. Please contact us:



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