

Reverse Costing analysis



SemiSouth SJEP170R550 1700V 550mOhm Vertical JFET

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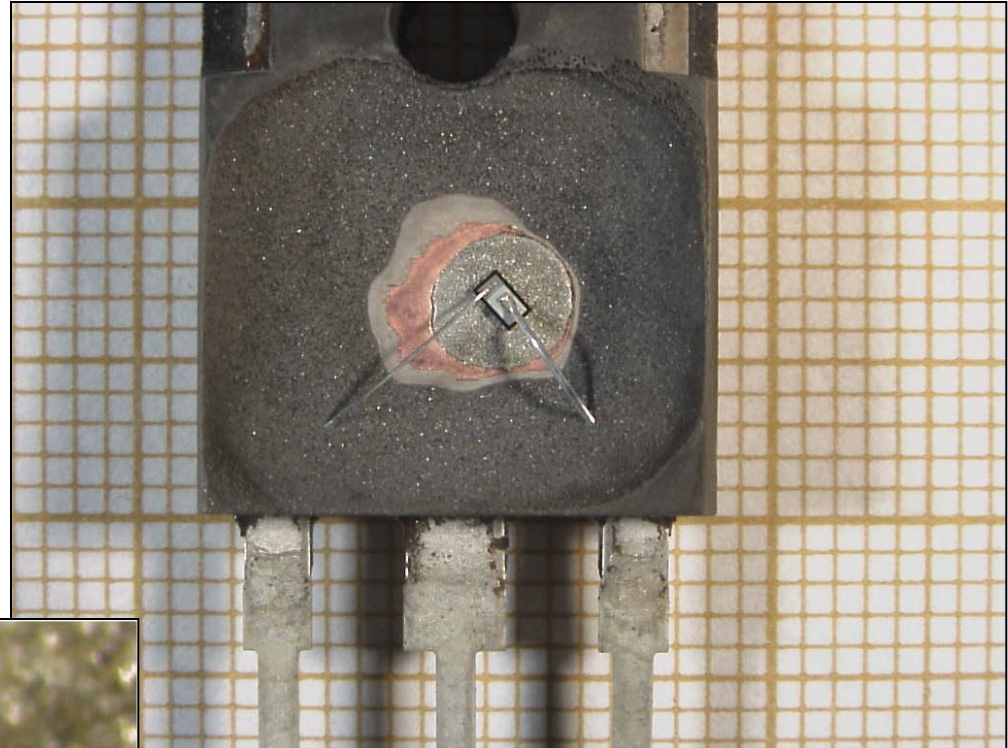
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Physical Analysis Methodology		Wafer Cost per process steps	
Package		Equipment Cost per Family	
Die Overview		Material Cost per Family	
Passivation		Die per Wafer and Probe Test	
Metal Layer		Probe Test	
JFET Transistor		Dicing and Package	
Substrate and epitaxy		Final Test Cost	
Back Side		JFET Die Cost	
Thickness Synthesis		Yields synthesis	
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Wafer Fabrication Unit			

Die in the TO247 after acid etching.

2 Aluminum wire bonds :

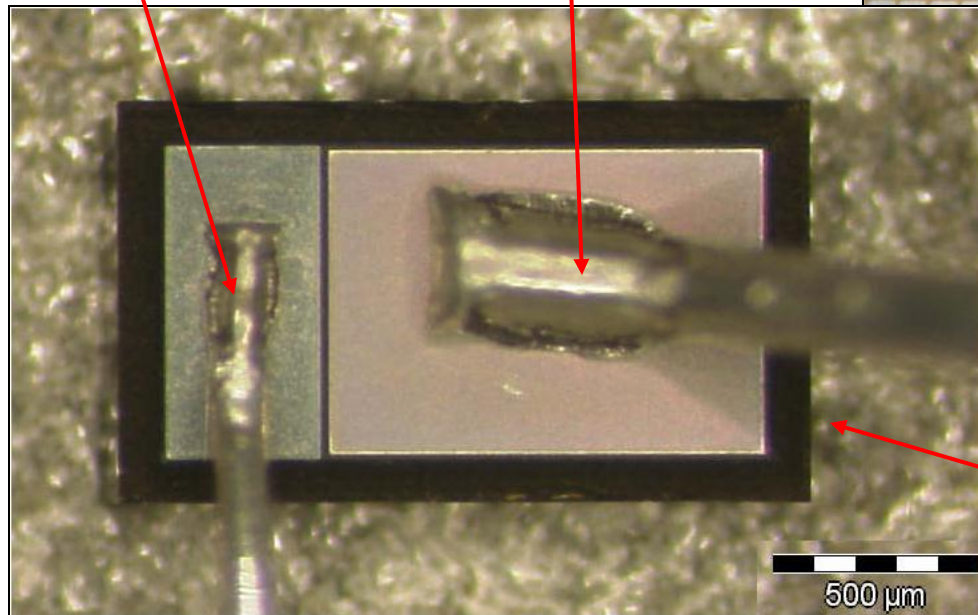
Gate bond : 6mm and 125 μ m of diameter.

Source bond : 8mm and 250 μ m of diameter.



Gate bond

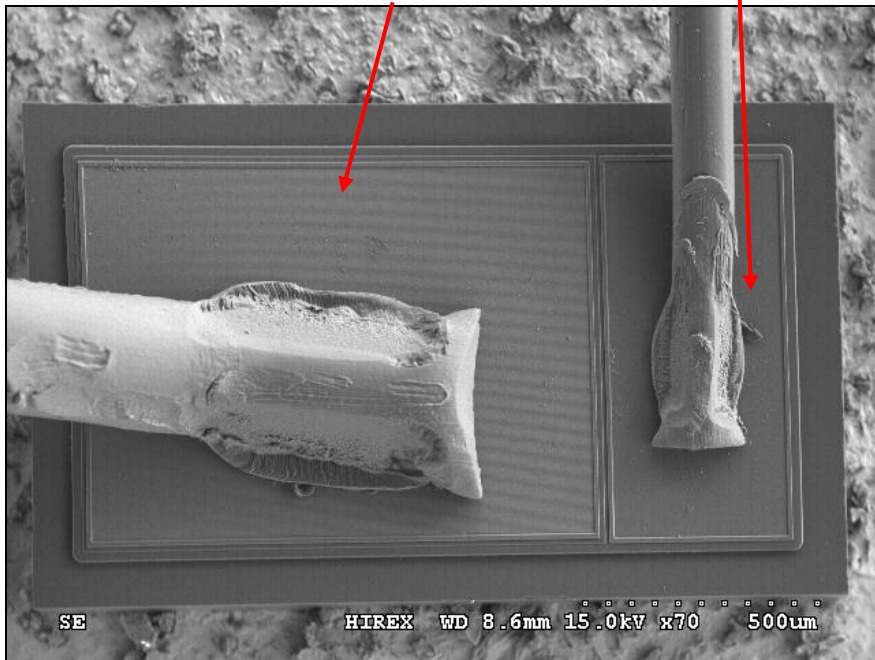
Source bond



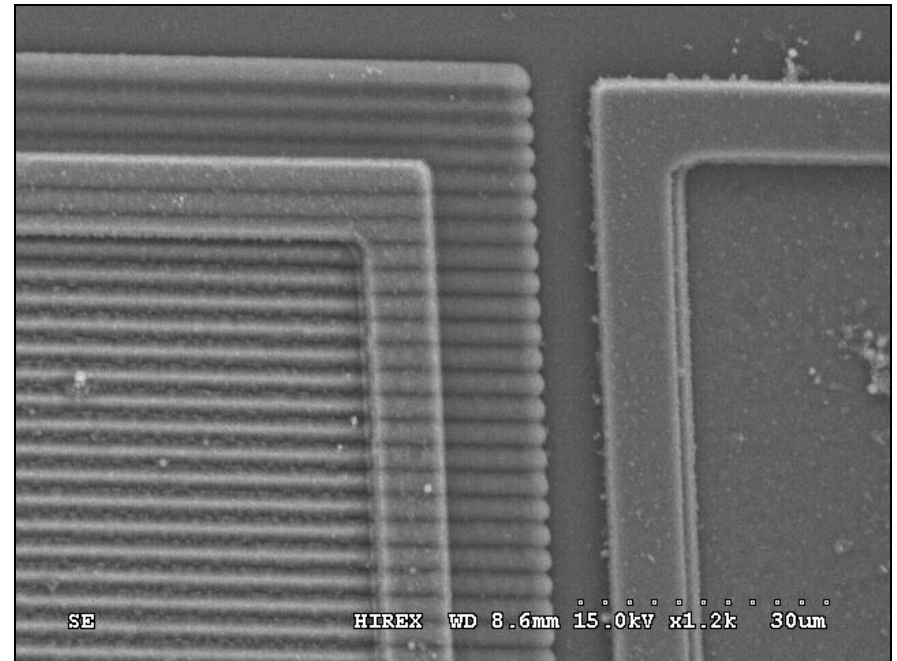
The Drain is directly soldered on the package leadframe with Sn solder.

Emitter area

Gate pad



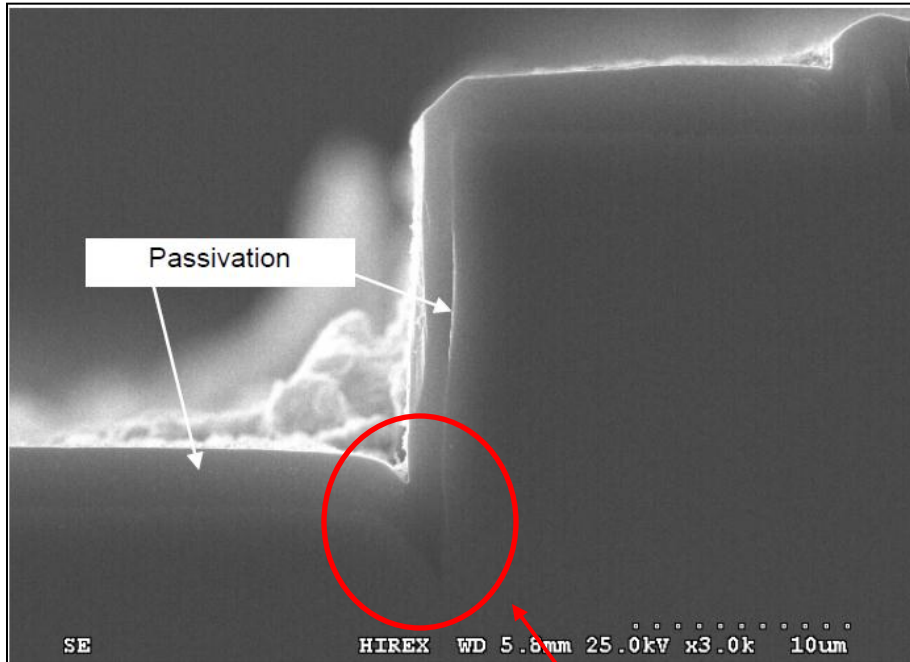
JFET die with the aluminum layer



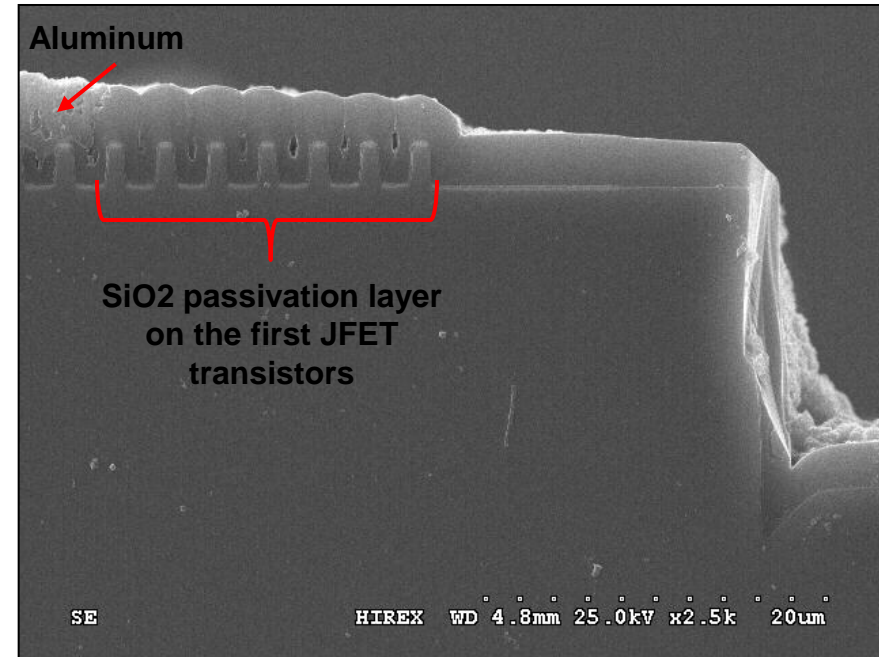
SEM picture : details.

JFET die cross section

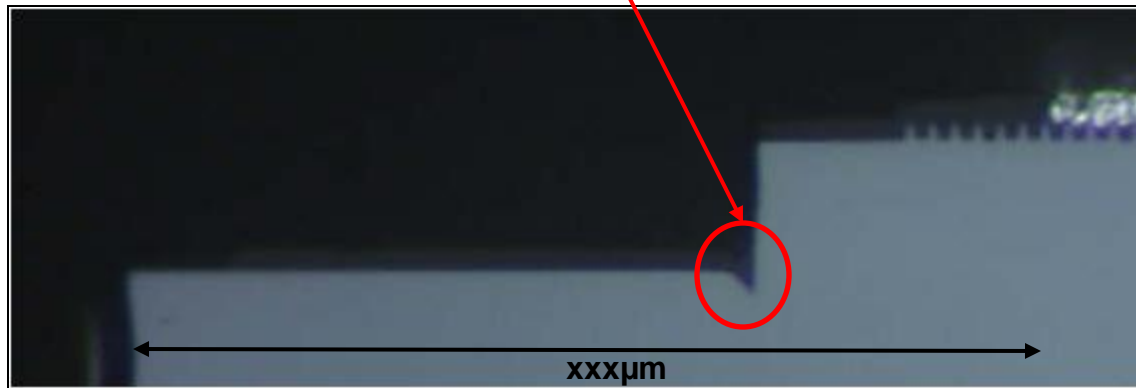
SEM view : Passivation details



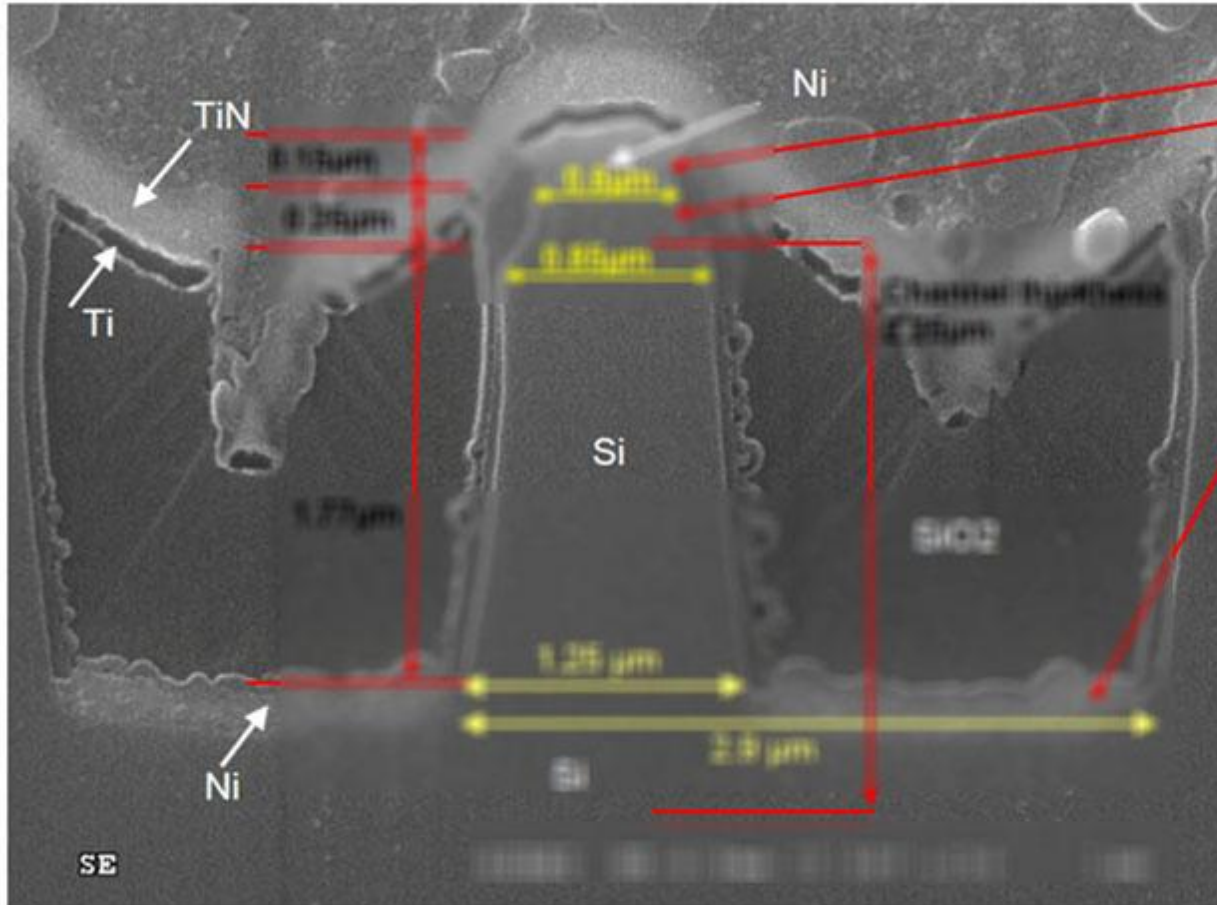
SEM view : Passivation details



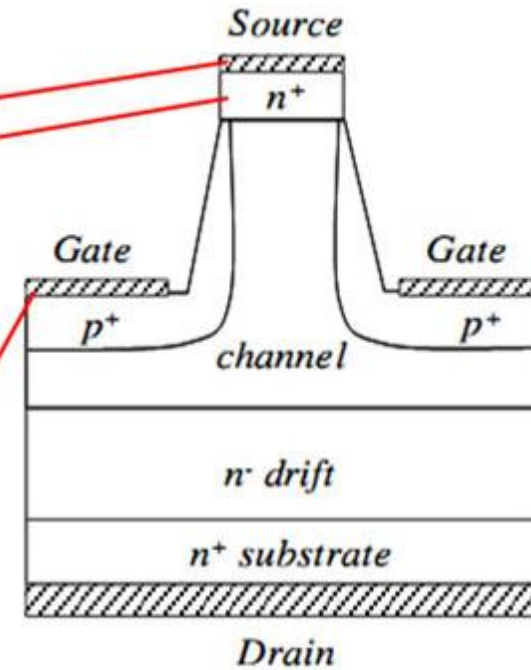
The fast plasma etching technique used to manufacture the MESA generates a hole at the base of the MESA



The protective area on the edges of the die is of XXXµm.

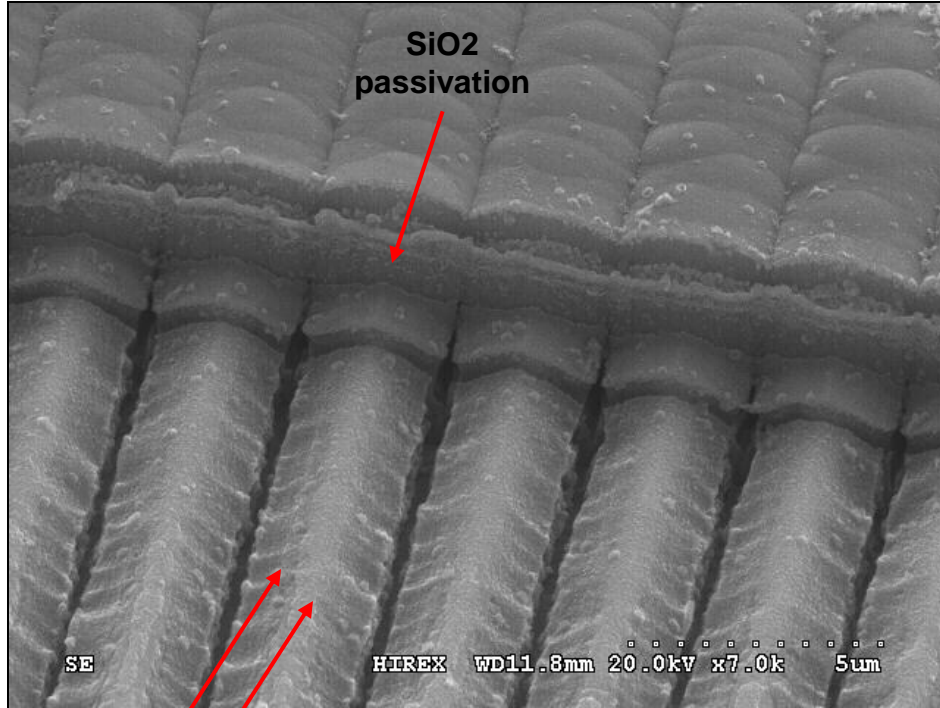


SEM view : JFET transistor

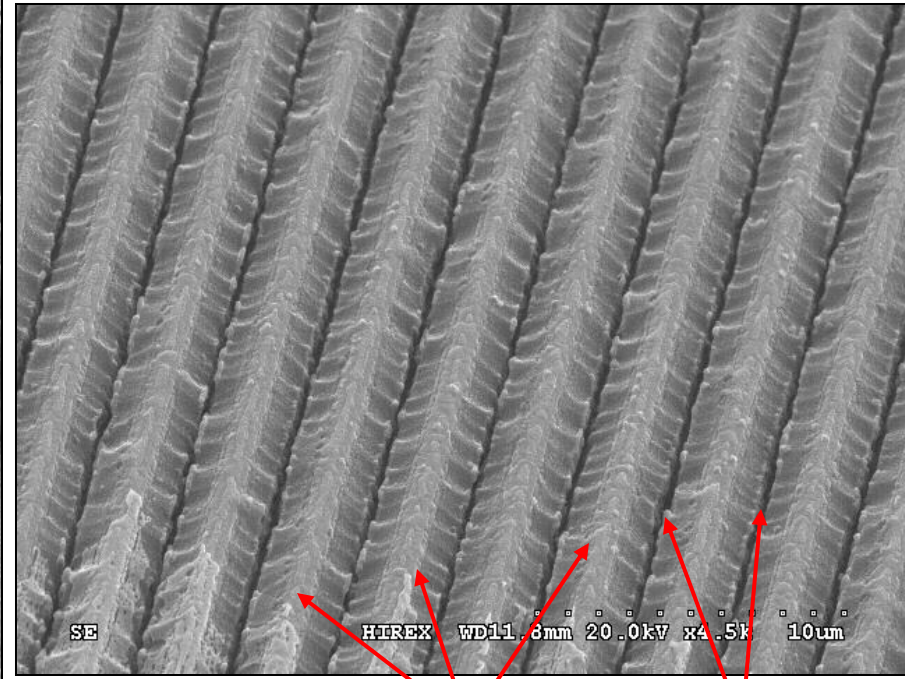


The standard revealed junction technique don't work on the SiC. Therefore we can not identify doping areas and the epitaxy thicknesses. We estimate the channel layer thickness at 2.25µm.

SEM view : JFET die without aluminum



Source pad (Without Aluminum ayer)



Source

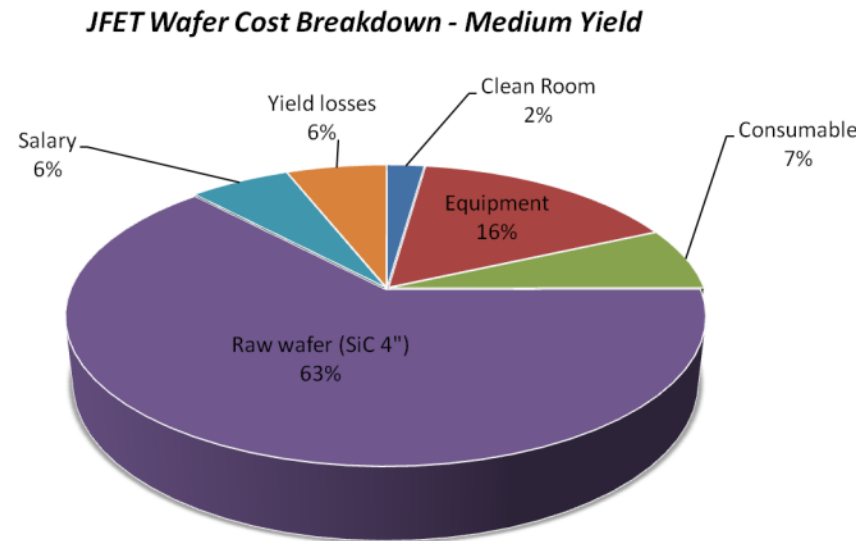
Gate

Cleaning	}	The substrate is etched. A first layer called buffer is deposited and then the diff region of 17µm is etched. The channel area and the source are then deposited.
SiC Epitaxy 20.5µm		
Wet-etching	}	A thick implant mask in SiO ₂ is deposited. An etching mask in nickel is deposited and patterned.
Cleaning		
TEOS deposit	}	The SiO ₂ implant mask is etched and the first nanometers of SiC are also etched. A control step is used in the process to enhance the accuracy.
N Deposition		
1 Pattern	}	A specific resin is used to etch the slope sidewall structure. The plasma etching is realized through this resin and gives this form. The channel is done.
N Etching		
PE Removal	}	The gate doping, the aluminum, is implanted in the gate zone. The wafers are heated at more than 700°C during the implantation to limit the crystal damages. Because of the increase and decrease of temperature, the duration of implantation is longer than usual.
BE Oxide		
Wet-etching	}	The sidewalls of the n ⁺ source are etched.
ICP RE SiC		
Slope etching resin deposit	}	The first oxide layer is deposited by CVD. Silane, NO and hydrogen gas are used for this deposition.
2 Pattern		
ICP RE SiC	}	
PE Removal		
Cleaning	}	
Wet-etching		
Implant Aluminum	}	
WETA		
Wet-etching	}	
N Etching		
Buffer oxide Etch	}	
Cleaning		
3 Pattern Source etching	}	
ICP RE SiC		
PE Removal	}	
Cleaning		
Wet-etching	}	
First SiO ₂ deposit		
Annealing		

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Clean Room	\$200,000	2.2%	\$200,000	2.2%	\$200,000	2.2%
Equipment	\$2,040,750	16.2%	\$2,040,750	16.2%	\$2,040,750	16.2%
Consumable	\$1,000,000	6.7%	\$1,000,000	6.7%	\$1,000,000	6.0%
Raw wafer (SiC 4")	\$2,440,000	62.7%	\$2,440,000	62.7%	\$2,440,000	62.7%
Salary	\$200,000	4.0%	\$200,000	4.0%	\$200,000	4.1%
Yield losses	\$1,000,000	7.0%	\$200,000	4.0%	\$700,000	5.0%
TOTAL	\$9,120,750		\$9,120,750		\$9,120,750	
Fab Yield	10.0%		10.0%		10.0%	

- The main part of the wafer cost is due to the raw wafer (XX%).
- The manufacturing yield is around XX% in 2010.

Details of the cost per step are given in the Excel Spreadsheet



	Final component cost	Floor price	Manufacturer price
2010 - Low Yield	\$0.170	\$0.177	\$0.185
2010 - Medium Yield	\$0.168	\$0.175	\$0.183
2010 - High Yield	\$0.166	\$0.173	\$0.181

Note: These calculated selling prices are for large quantities purchased directly from SemiSouth.

