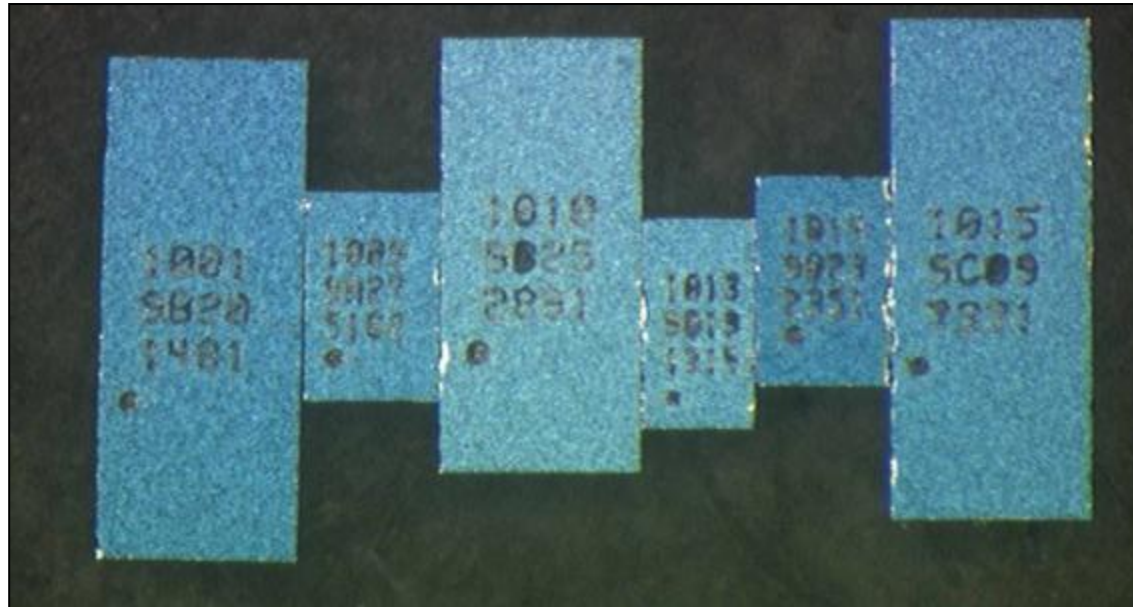


# Reverse Costing analysis



## Efficient Power Conversion GaN transistors (EPC 1001 – 1009 – 1010 – 1013 – 1014 - 1015)

July 2010 - Version 1

Written by: Sylvain Hallereau

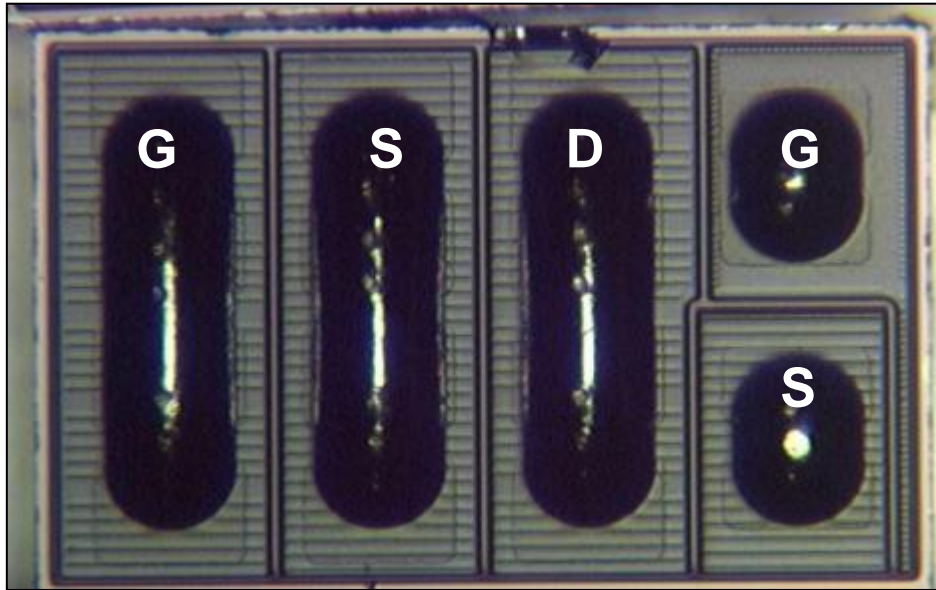
DISCLAIMER : System Plus Consulting provides cost studies based on its knowledge of the manufacturing and selling prices of electronic components and systems. The given values are realistic estimates which do not bind System Plus Consulting nor the manufacturers quoted in the report. System Plus Consulting is in no case responsible for the consequences related to the use which is made of the contents of this report. The quoted trademarks are property of their owners.

<b>Glossary</b>	
<b>1. Overview / Introduction.....</b>	<b>4</b>
– Executive Summary	
– Reverse Costing Methodology	
<b>2. EPC Company Profile.....</b>	<b>8</b>
<b>3. Physical Analysis.....</b>	<b>12</b>
– Synthesis of the physical analysis	
– Physical analysis methodology	
– GaN-Si structure	
– Package characteristics & markings	
– Package opening	
– Semiconductor Die	
– Plan view analysis	
– Cross section analysis	
– Back end process (optical and SEM)	
– Front end process (SEM and TEM)	
– Summary of process parameters	
– Device Dimensions	
– 1001	
– 1009	
– 1010	
– 1013	
– 1014	
– 1015	
– Devices Summary table	
– Device Layout	
<b>4. DC electrical parameters .....</b>	<b>49</b>
– V <sub>th</sub>	
– I <sub>Gss</sub>	
– I <sub>Dss</sub>	
<b>5. Manufacturing Process Flow.....</b>	<b>53</b>
– Overview	
– GaN-Si process flow	
– Description of the Wafer Fabrication Unit	
<b>6. Cost Analysis.....</b>	<b>68</b>
– Synthesis of the cost analysis	
– Main steps of economic analysis	
– Yields explanation	
– Wafer cost	
– Breakdown per Step	
– Breakdown per Equipment	
– Breakdown per Consumable	
– Probe Test cost	
– Dicing and Final Test Cost	
– Component Manufacturing Cost	
– 1001	
– 1009	
– 1010	
– 1013	
– 1014	
– 1015	
– Yields synthesis	
<b>7. Estimated Manufacturer Price Analysis.....</b>	<b>88</b>
– Supply Chain Analysis	
– Manufacturer ratios	
– Estimated manufacturer Price	
<b>Conclusion .....</b>	<b>97</b>

The devices subject to teardown for this work are six EPC enhancement mode gallium nitride on silicon power transistors. Six devices are analyzed. The devices are sold as solder-bumped bare dice.

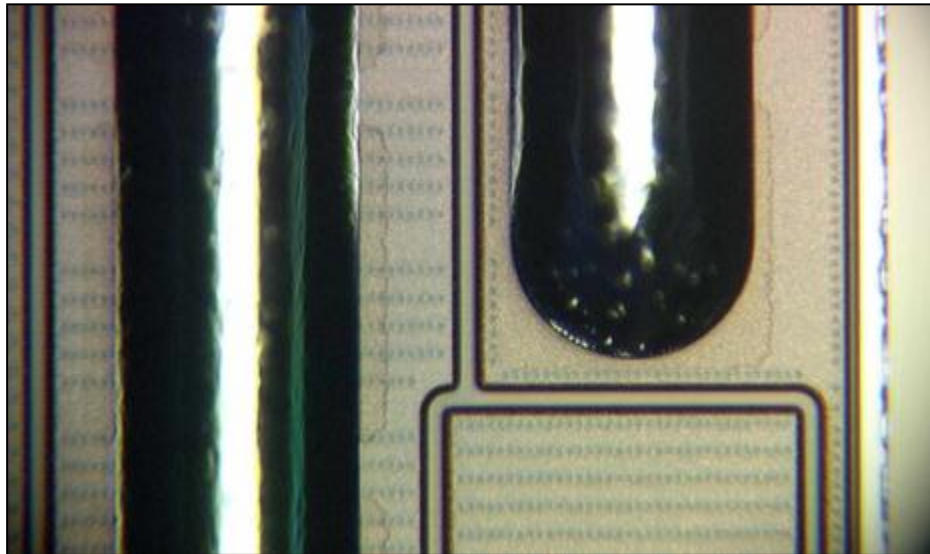
## Devices analyzed

EPC device	V rating	Rmax (mOhm)	Die size (mmxmm)	Markings line 2	Markings line 3
1015	40	4	4.1x1.6	9C09	7333
1014	40	16	1.7x1.1	9?23	2353
1013	150	100	1.7x0.9	9D13	1321
1010	200	27	3.6x1.6	9B25	2893
1009	60	30	1.7x1.1	9B22	5164
1001	100	7	4.1x1.6	9B20	1481



*Device 1009.*

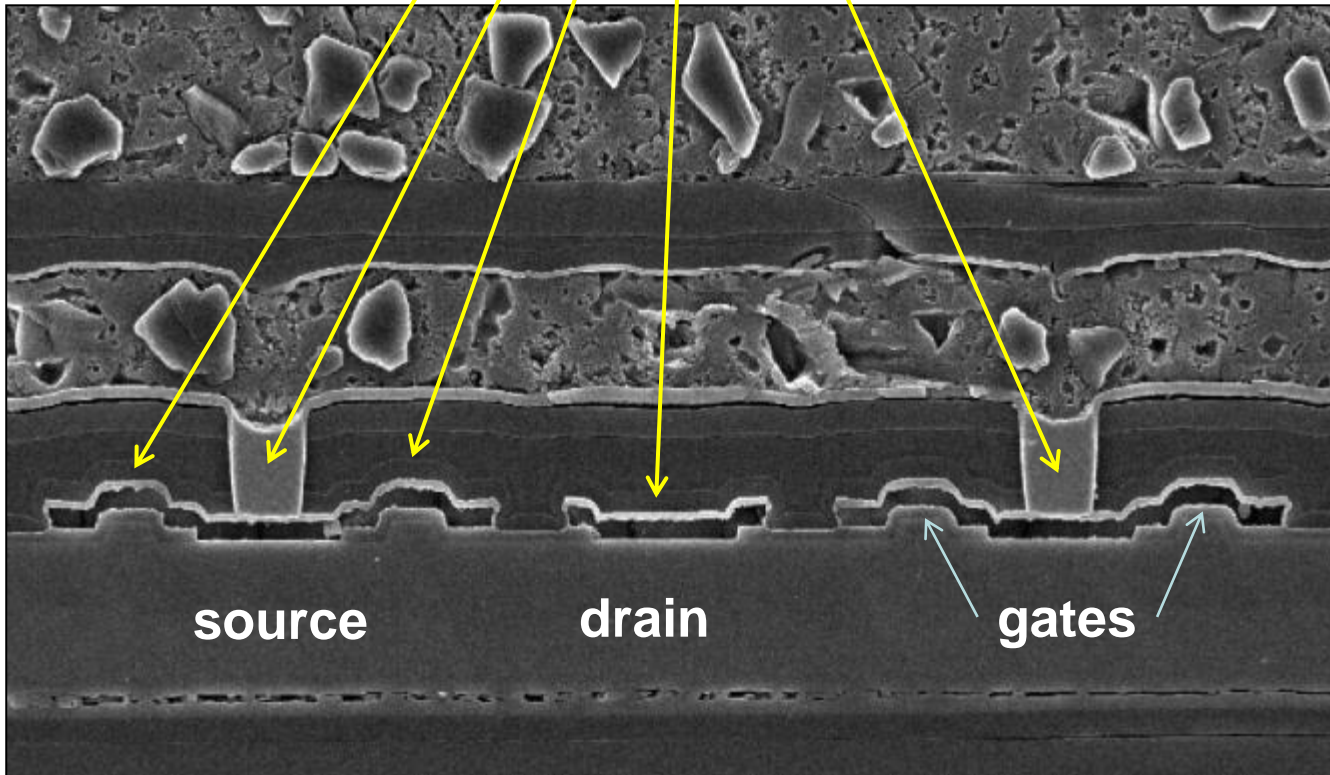
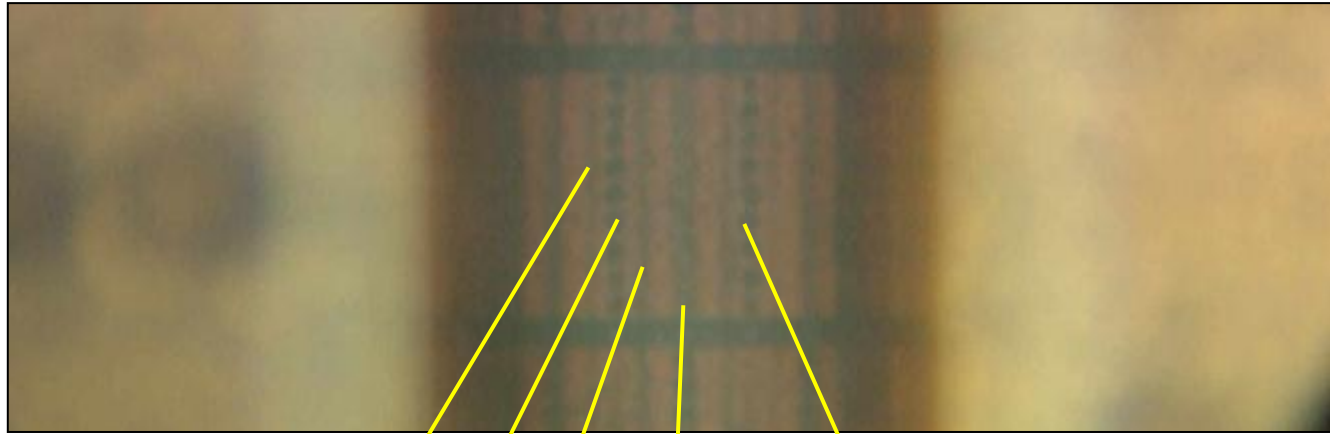
*All devices are built in the same way. Longer devices have more alternating S-D solder bumps.*



*There are three layers of metals, plus the solder bumps.*

*Each solder bump lies on a Metal 3 plate, connecting to Metal 2 by rows of contacts.*





M3

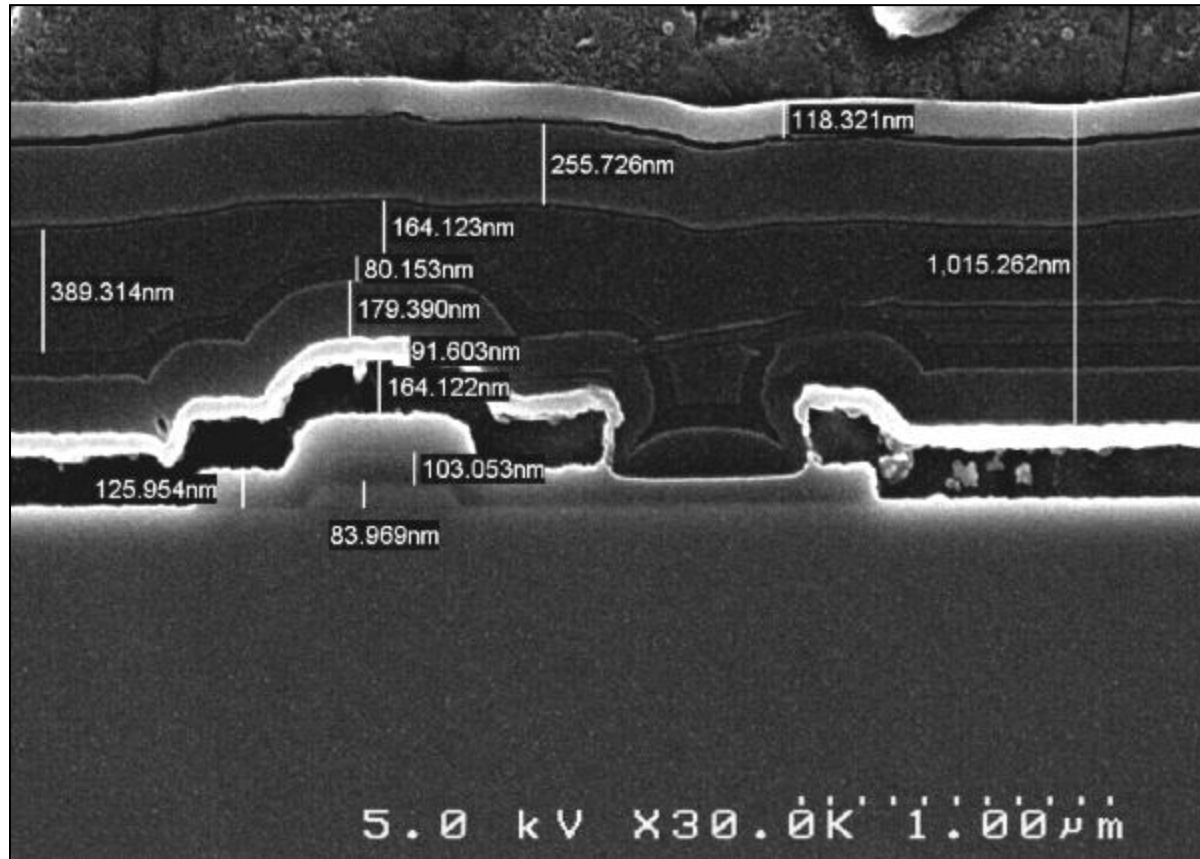
M2

M1

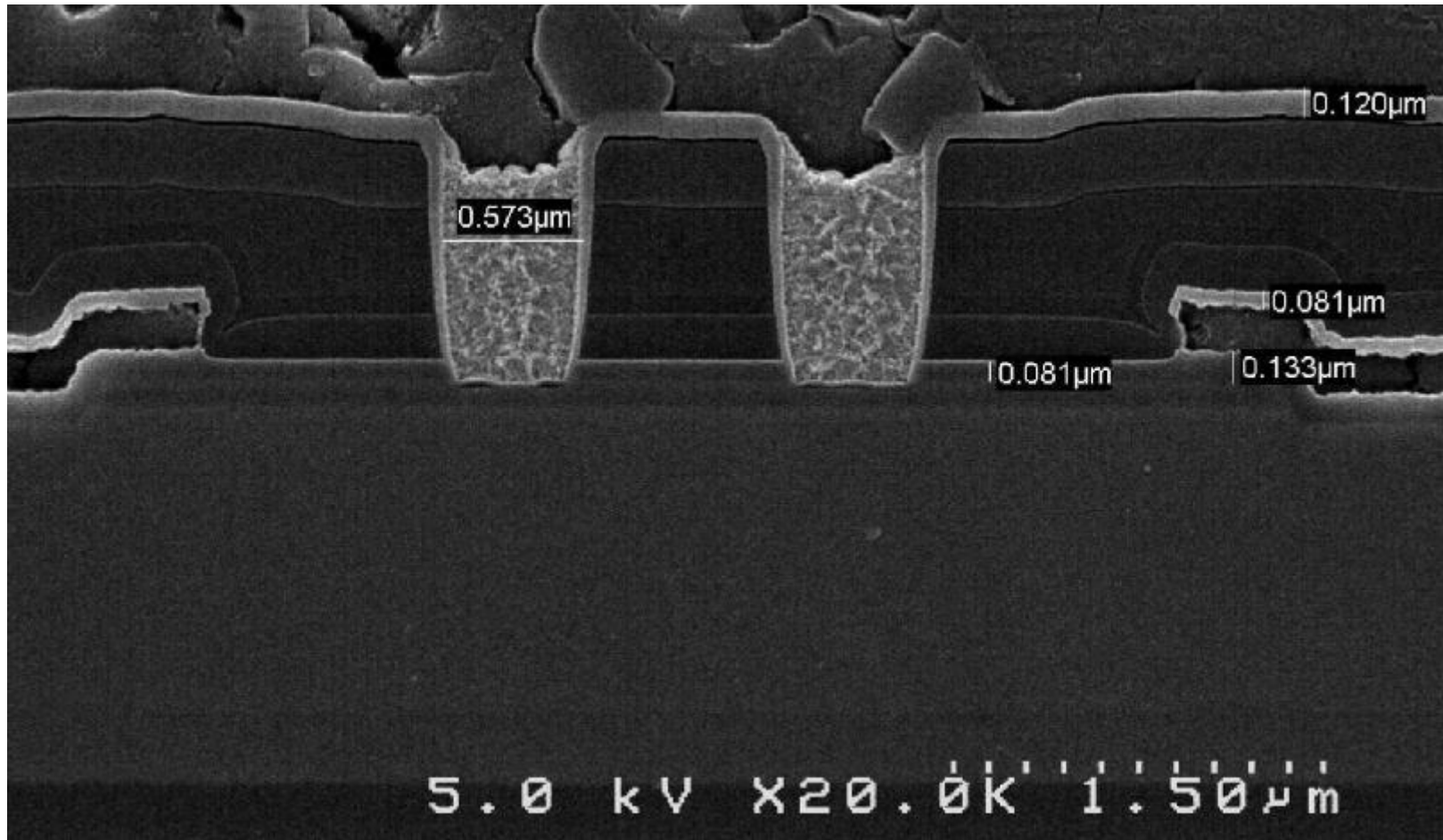
source

drain

gates

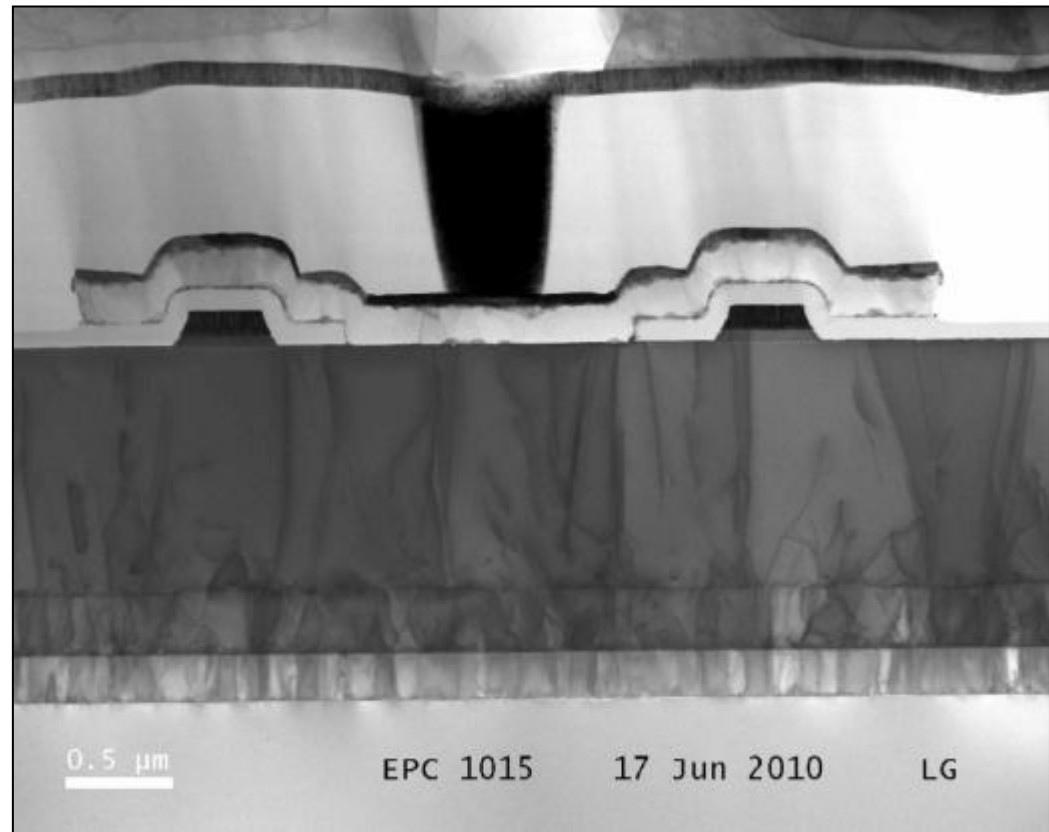
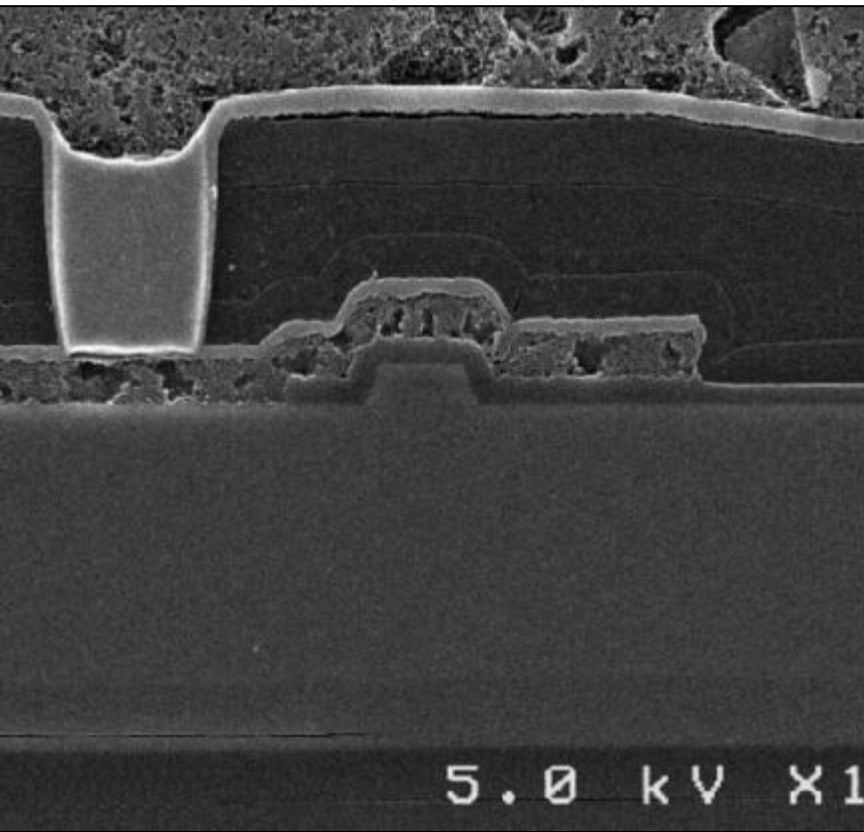


*Details of the intermetal dielectric between Metal 1 and Metal 2. After the patterning of M1, a highly conformal oxide is deposited, creating re-entrant corners. Layers of what appears to be spin-on-glass are used to restore planarity before the vias are opened for the tungsten plugs and the subsequent deposition and patterning of the die-length Metal 2 strips.*



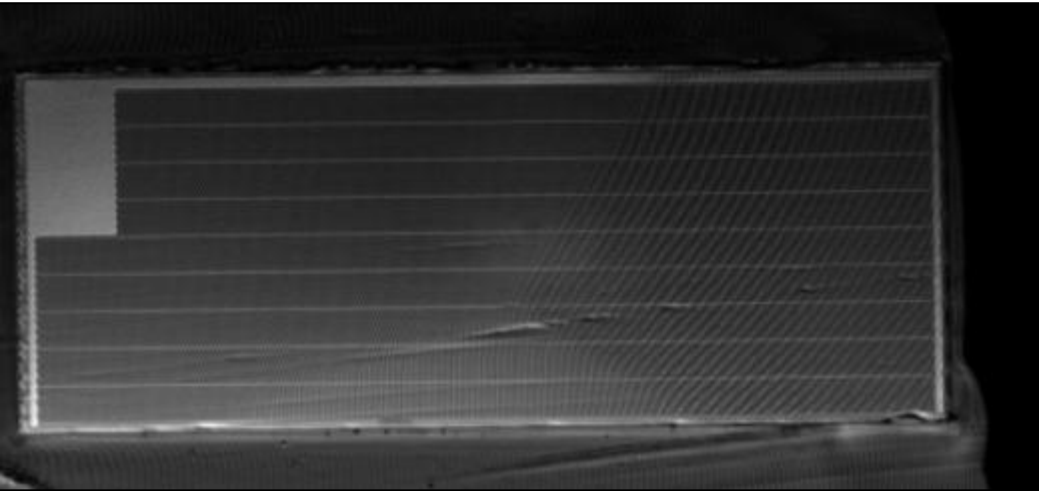
*The W plugs are 0.5µm in diameter.*



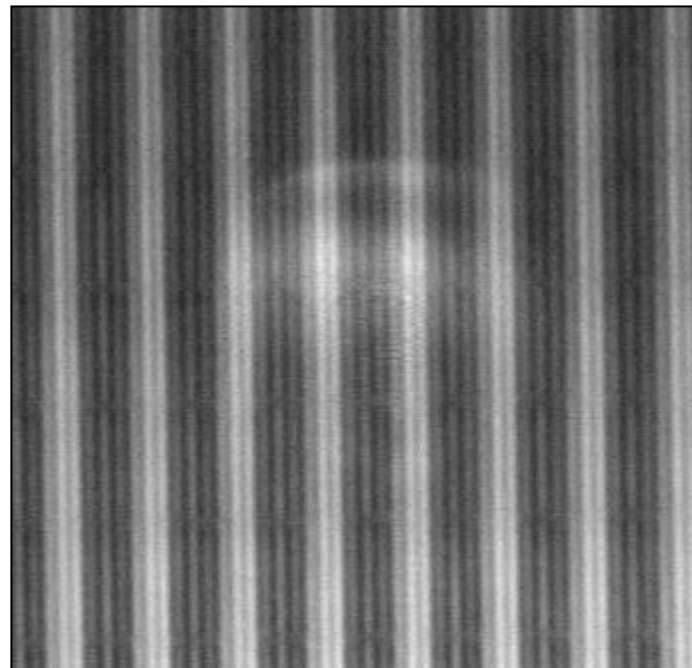
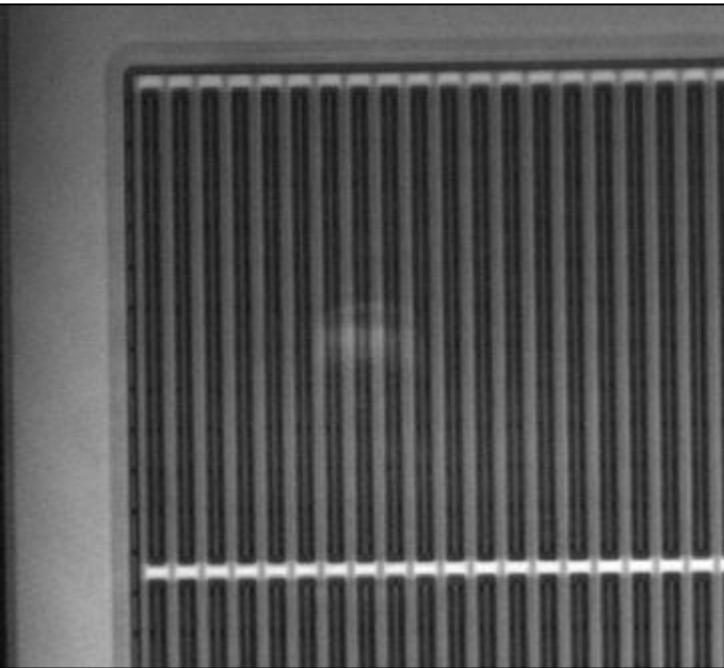


*Higher magnification SEM (left) and TEM (right) cross-section view of transistors and the GaN layers*





*General overview of device 1001. The white rectangle is the gate contact pad. The horizontal white lines are gate contacts.*



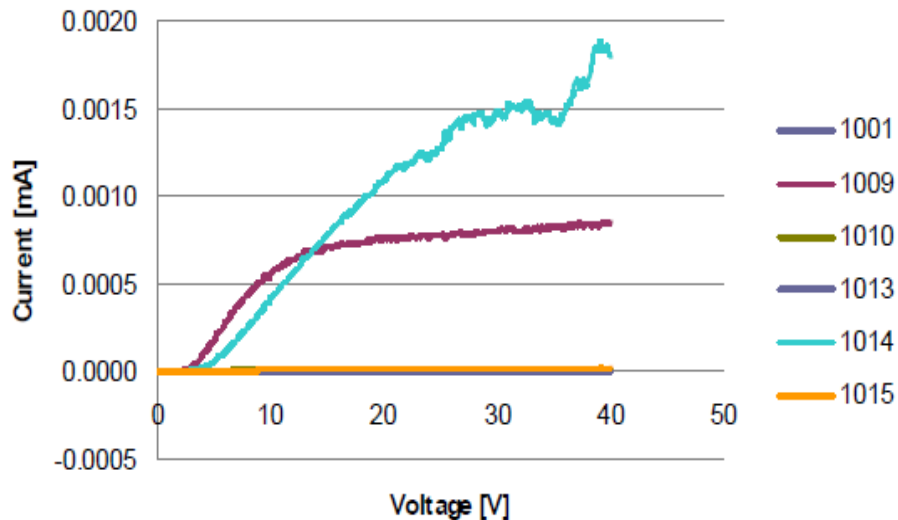
*Images with the 50x objective. Zoom 1 (left) and zoom 3 (right).*

*The thin white lines are the source contact; the fatter gray lines are the drain contacts. Individual gates are not resolved.*

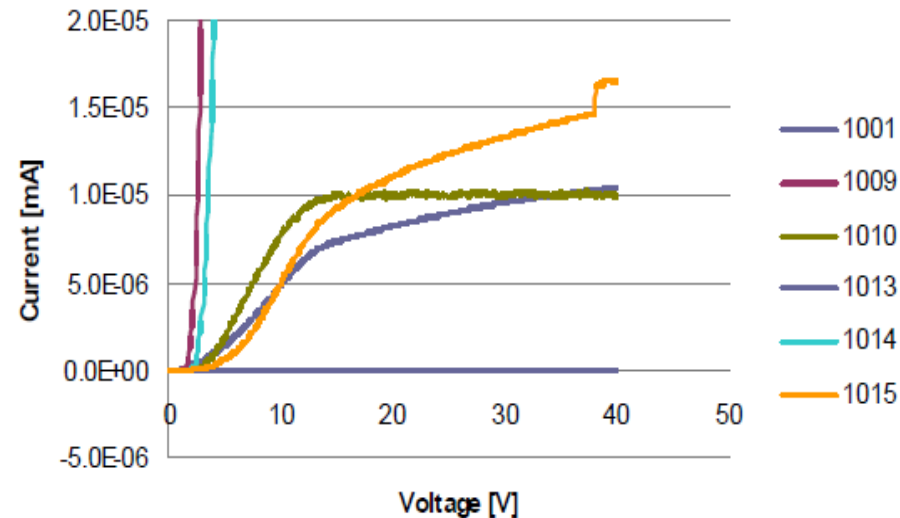
## IDss

For this measurement the Gate is tied to the Source ( $V_{GS}=0$ ) and  $V_D$  swept from 0V to 40V measuring Drain current. Both graphs show the same data but with different vertical scales.

### IDSS measurement



### IDSS measurement



- Transistor**
- Inspection
  - Cleaning
  - Deposit TiN - 100nm
  - Measurement Thickness
  - Cleaning
  - 1 - Pattern Gate
  - Etching TiN - 100nm
  - Etching GaN - 85nm
  - PE Removal
  - Measurement
  - Cleaning
  - Deposit Si3N4 - 125nm
  - Cleaning
  - 2 - Pattern Si3N4
  - Measurement
  - Etching Si3N4 - 125nm
  - PE Removal
  - Cleaning
  - Deposit Aluminum + TiN - 100nm + 30nm
  - Cleaning
  - Measurement Thickness
  - 3 - Pattern Metal 1
  - Etching TiN - 30nm
  - Etching Aluminum - 100nm
  - Measurement
  - PE Removal
  - Cleaning
  - Deposit Oxide 1 - SiO2 180nm
  - Deposit Oxide 2 - SiO2 80nm
  - Cleaning
  - Measurement Thickness
  - Deposit Oxide 3 - SiO2 280nm
  - Baked SiO2
  - Deposit Oxide 4 - SiO2 280nm
  - Baked SiO2
  - Annealing SiO2
  - Cleaning
  - Measurement Thickness

## The main parts of the process:

### Transistor

- (1) The Tin layer is deposited and the gate is patterned.
- (2) A shield in Si3N4 is deposited and patterned to protect the gate.
- (3) The metal 1, the Drain and Source electrode are deposited directly in contact with the GaN.
- (4) The IMD is realized by a SOG technique.

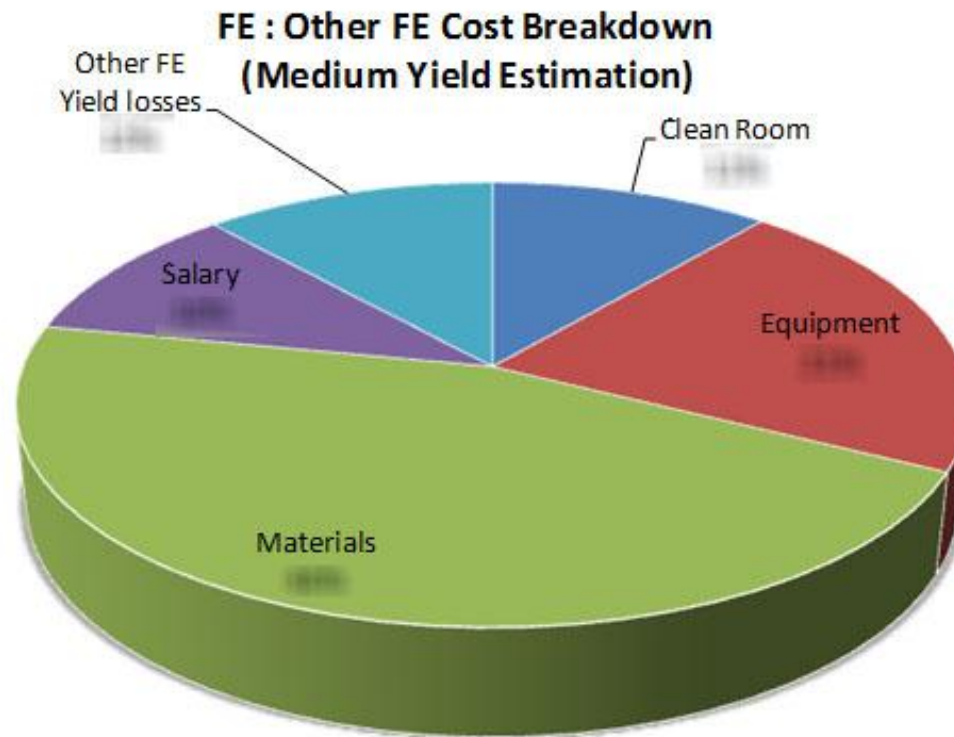
### Metal Layers

- (1) The vias between the metal 1 and metal 2 are etched and filled with tungsten.
- (2) The Metal 2 is deposited and patterned.
- (3) The IMD 2 is deposited and the vias between the metal 2 and metal 3 are etched.
- (4) The metal 3 is deposited and patterned.
- (5) The passivation layers (SiO2 + Si3N4) are deposited.
- (6) The pad are opened.

### Metal Layers

- 4 - Pattern Plug HCl
- Etching SiO2 - 1µm
- Cleaning
- Measurement
- PE Removal
- Deposit TiN - 100nm
- Deposit W - 1.5µm
- Etching W - 1.5µm
- Cleaning
- Measurement
- Deposit Metal 2 - Aluminum/TiN - 1.5µm
- Cleaning
- 5 - Pattern Metal 2
- Etching Metal 2
- Measurement
- PE Removal
- Cleaning
- Deposit HfO2 - SiO2 280nm
- Baked SiO2
- Deposit HfO2 - SiO2 280nm
- Baked SiO2
- Annealing SiO2
- Measurement Thickness
- Cleaning
- 6 - Pattern Plug HCl
- Etching SiO2 - 1.5µm
- PE Removal
- Cleaning
- Measurement
- Deposit Aluminum - 4.5µm
- Cleaning
- 7 - Pattern Metal 3
- Etching Metal 3
- PE Removal
- Cleaning
- Measurement
- Deposit Oxide Passivation - SiO2 1.800µm
- Deposit Si3N4 Passivation - 0.7µm
- 8 - Pattern Passivation
- Etching Passivation - 1.5µm
- PE Removal
- Cleaning
- Measurement

Total Front-End	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw Substrate Cost (Si)	1000000	10.0%	1000000	10.0%	1000000	10.0%
FE : Epitaxy Cost	1000000	10.0%	1000000	10.0%	1000000	10.0%
FE : Other FE Cost	1000000	10.0%	1000000	10.0%	1000000	10.0%
FE : Yield Losses Cost	1000000	10.0%	1000000	10.0%	1000000	10.0%
<b>TOTAL Front-End Cost</b>	<b>10000000</b>	<b>100%</b>	<b>10000000</b>	<b>100%</b>	<b>10000000</b>	<b>100%</b>





Die Cost	1001	1009	1010	1013	1014	1015
V rating	100V	60V	200V	150V	40V	40V
Id	25A	6A	12A	3A	10A	33A
Die Area (in mm <sup>2</sup> )	6.10E-0007	1.12E-0007	5.78E-0007	1.12E-0007	1.12E-0007	6.10E-0007
Low Yield	85.000	85.000	85.000	85.000	85.000	85.000
Medium Yield	85.000	85.000	85.000	85.000	85.000	85.000
High Yield	85.000	85.000	85.000	85.000	85.000	85.000

