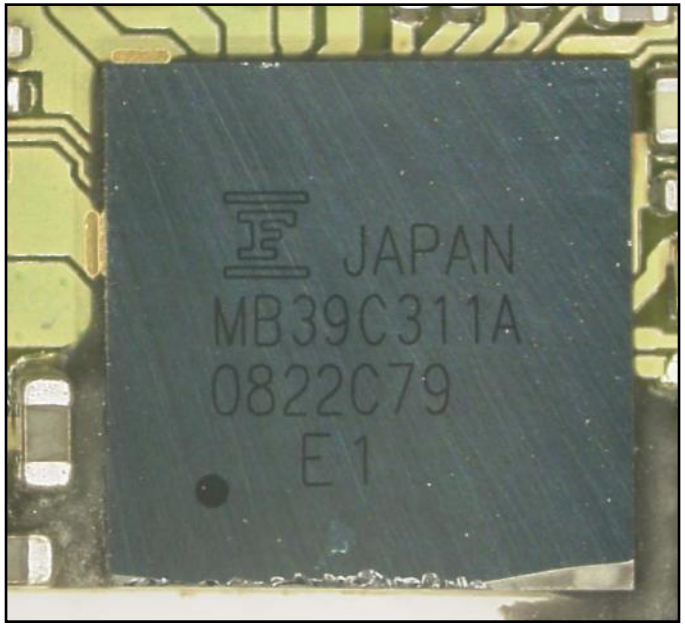
9 rue Alfred Kastler - BP 10748 - 44307 Nantes Cedex 3 - France
Phone : +33 (0) 240 180 916 - email : info@systemplus.fr - website : www.systemplus.fr

Reverse Costing analysis



EWLP 309-pin by Casio Micronics – Fujitsu MB39C311A
The largest Full Wafer Level Chip Scale Package

June 2010- Version 2

Written by: Sylvain HALLEREAU

DISCLAIMER : System Plus Consulting provides cost studies based on its knowledge of the manufacturing and selling prices of electronic components and systems. The given values are realistic estimates which do not bind System Plus Consulting nor the manufacturers quoted in the report. System Plus Consulting is in no case responsible for the consequences related to the use which is made of the contents of this report. The quoted trademarks are property of their owners.

© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

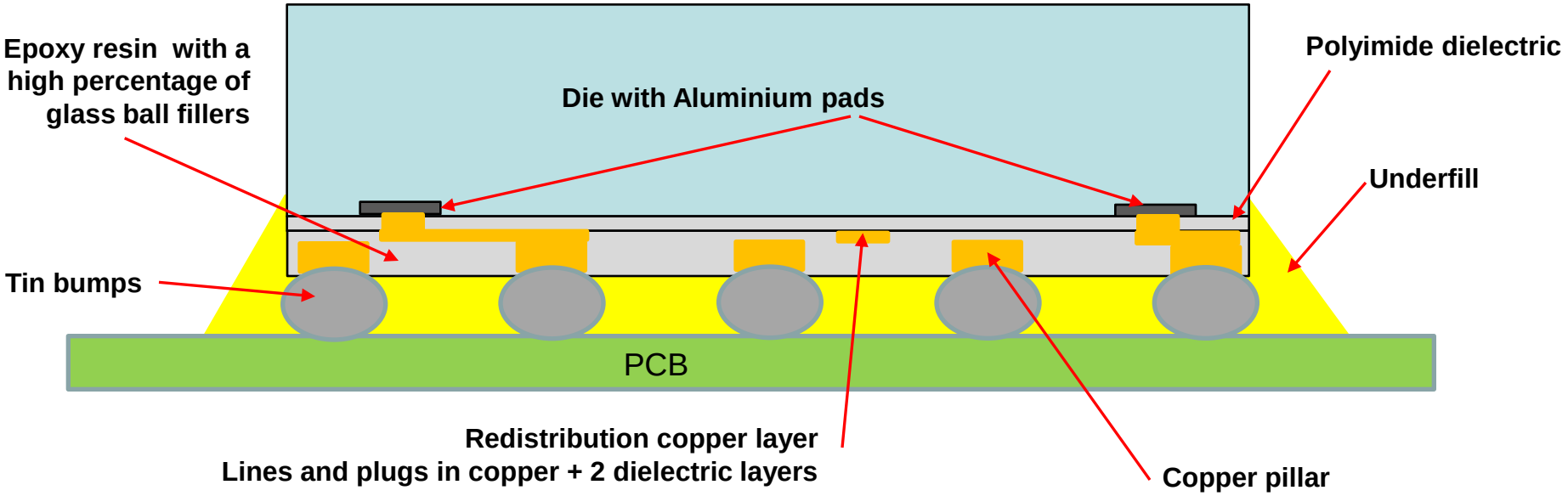
Table of Contents

© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

Physical Analysis Methodology

- **Package is analyzed and measured.**
  - **X-ray pictures are used to identify the package construction and the redistribution.**
- **One cross-section is realized to get overall package data : dimensions, main characteristics.**
- **Analysis of used technology and materials is provided.**

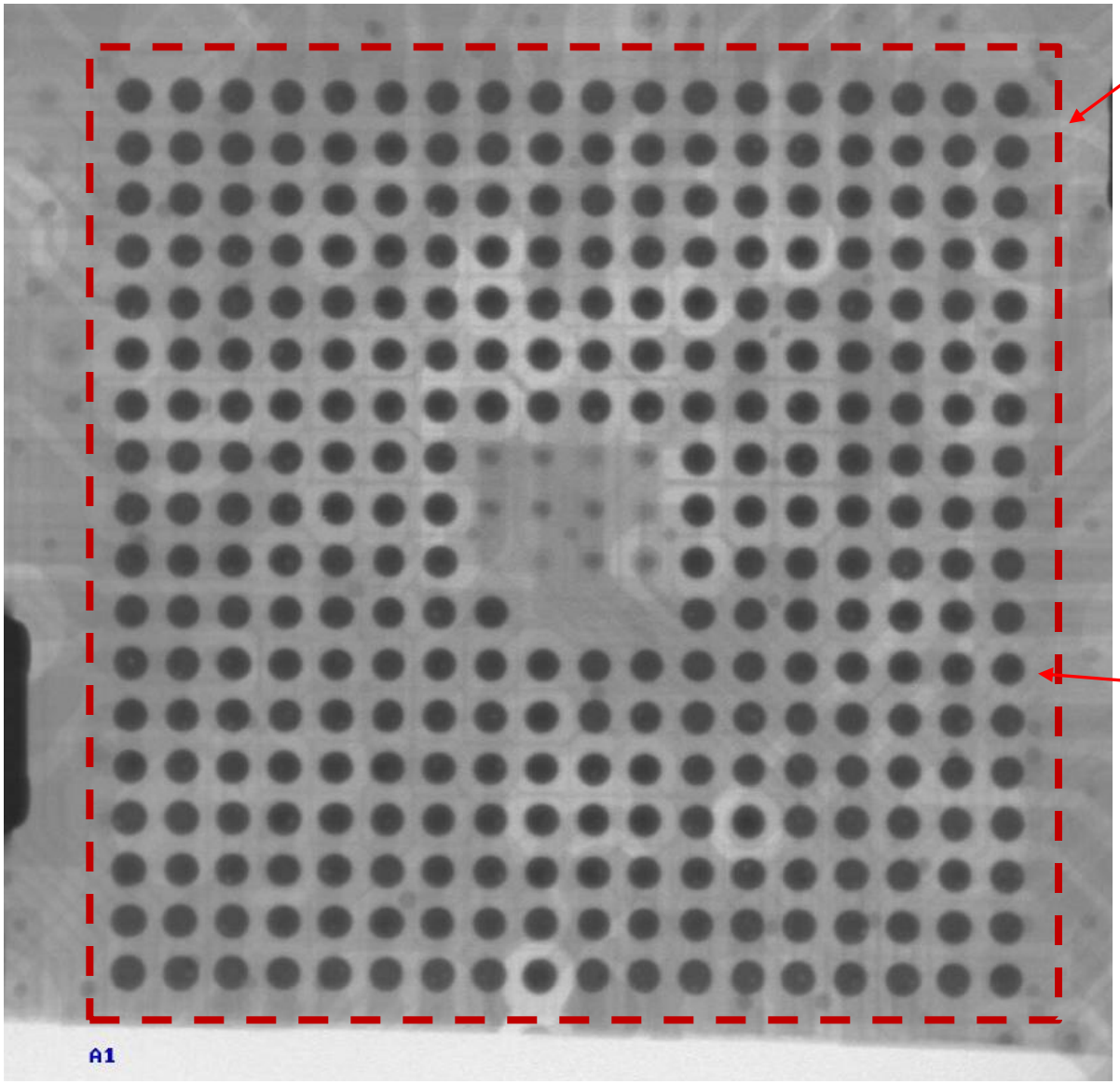
The schematic diagram below is based on the observations made during this study and detailed in the next slides.



© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

Die in the package

This X-Ray picture of WL-CSP with the PCB.



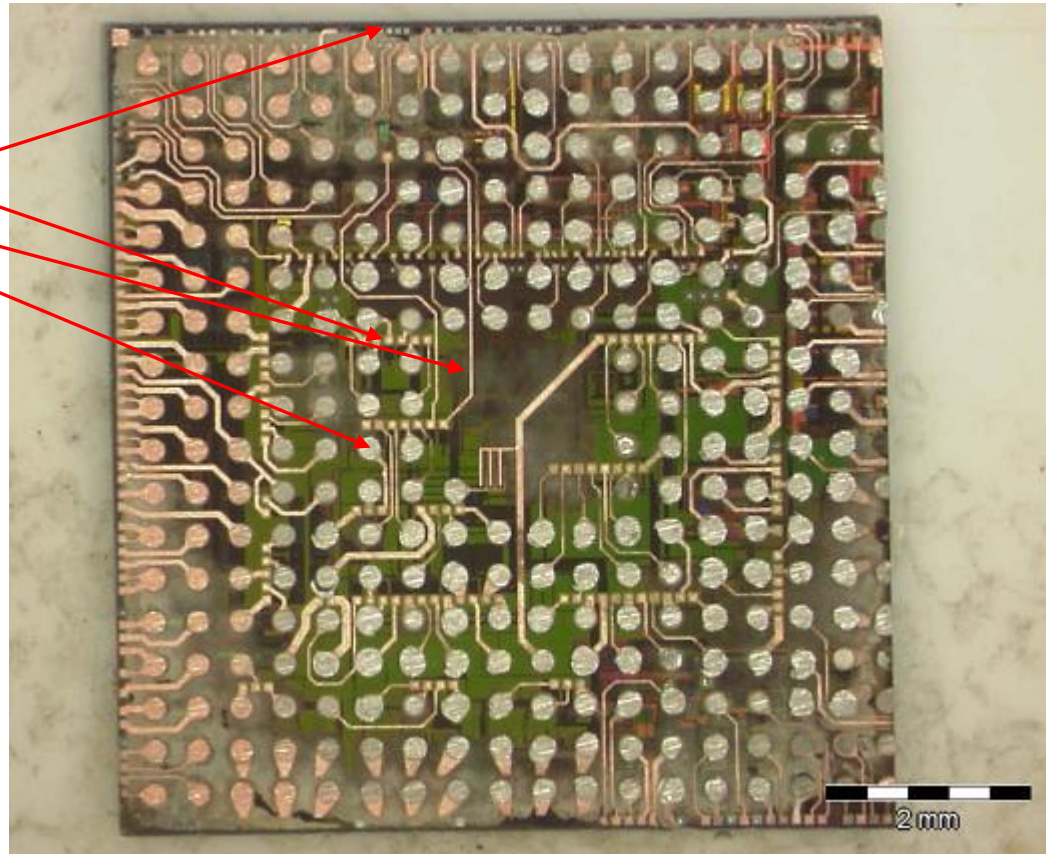
Die
7.45mm x 7.45mm = 55.5mm²

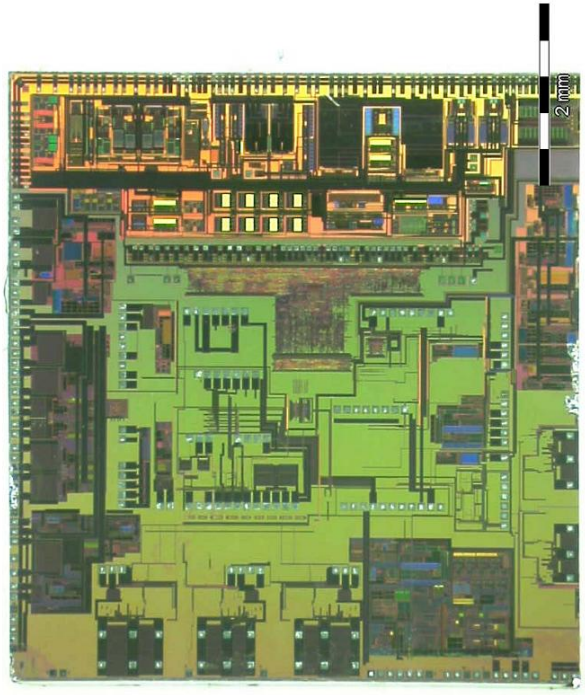
250µm between the side of the die and the first balls.

© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

Pads and redistribution layer

WL-CSP after underfill layer is removed. This picture shows the redistribution layer between the pads and the solder balls.



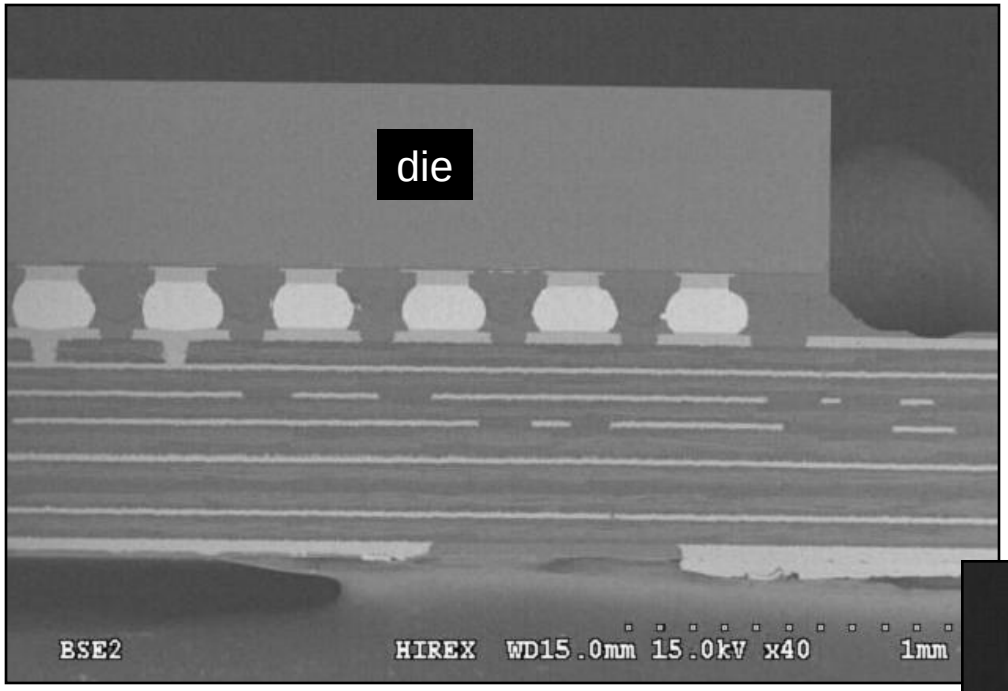


Die after redistribution layer removed.

Cross section cut

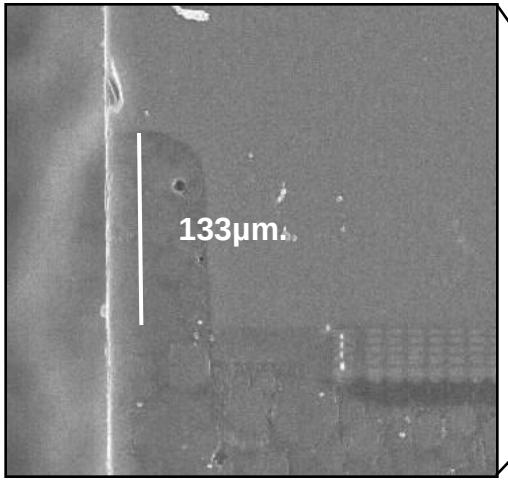
© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

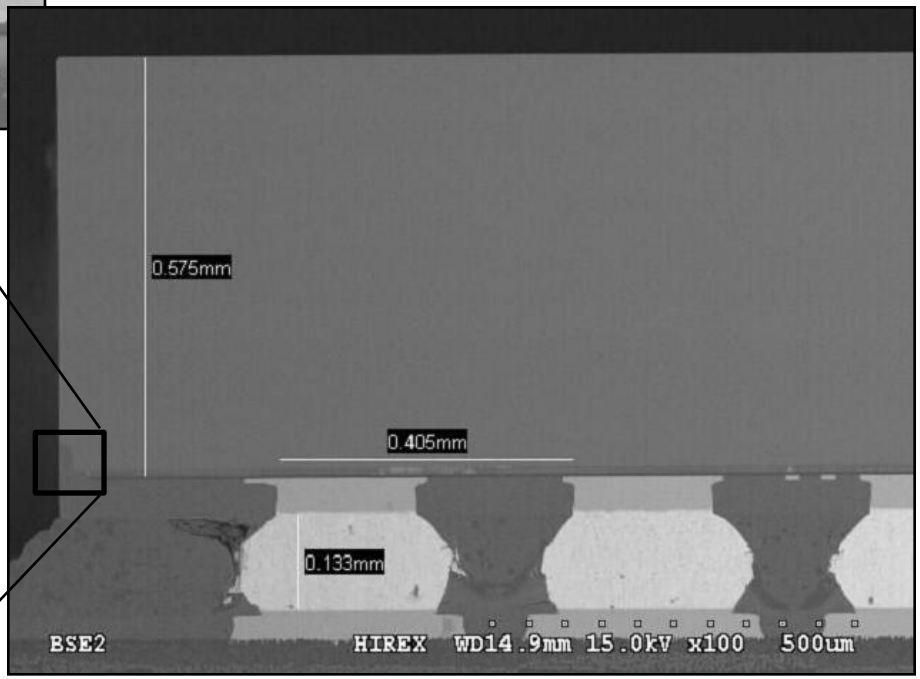
Bumps



A bump pitch is 400µm.

A Pre-saw is realized and filled with a dielectric in order to enhance the die protection.





© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

Redistribution

- WL-CSP
  - Additional BE - Cleaning
  - Additional BE - Measurement
  - Additional BE - Polyimide deposition (3µm)
  - Additional BE - Pattern
  - Additional BE - Cleaning
  - Additional BE - Measurement
  - UBM Barrier/Seed - TiN deposition
  - UBM Barrier/Seed - Cu PVD deposition
  - UBM Barrier/Seed - Reflow
  - UBM Barrier/Seed - Cleaning
  - UBM Barrier/Seed - Measurement
  - Redistribution layer - Deposition
  - Redistribution layer - Pattern
  - Redistribution layer - Cure thick resin
  - Redistribution layer - Cleaning
  - Redistribution layer - Measurement
  - Redistribution layer - Copper ECD 6µm
  - Redistribution layer - PR Removal
  - Redistribution layer - Cleaning

- The wafer is cleaned.

- A polyimide layer is deposited in order to increase the die protection against moisture and planarize the wafer.

- A thin barrier layer of titanium nitride is deposited.
- A thin Copper layer is deposited to serve as a seed layer.
- The mechanical stress is reduced by an annealing.

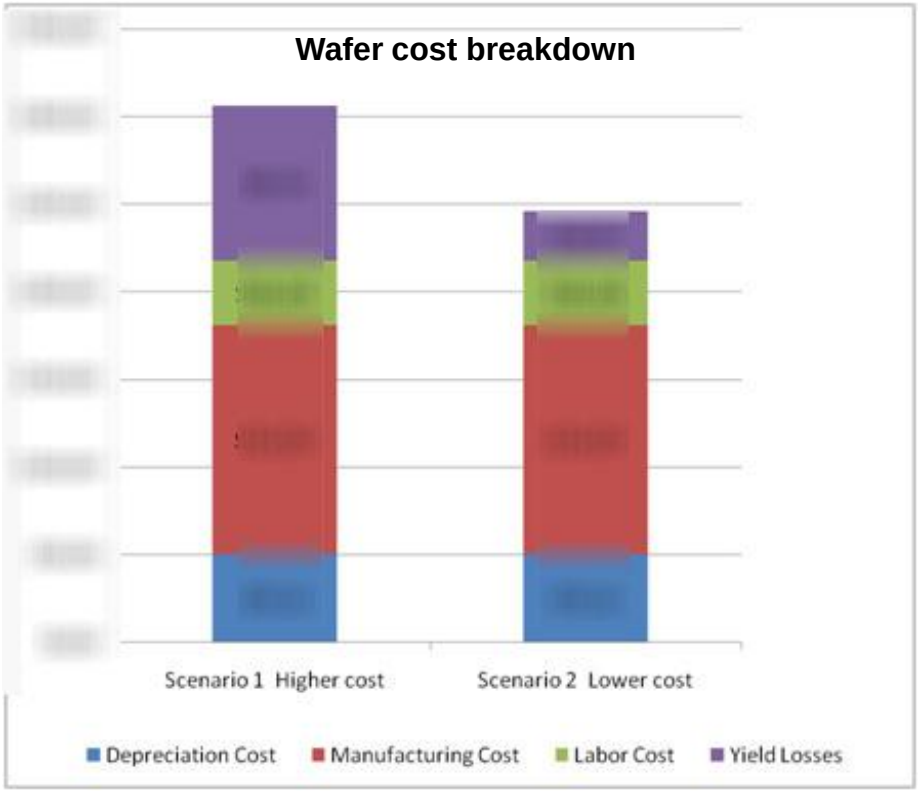
- A resin mask is patterned and the copper lines are electroplated.
- The development step is integrated in the Deposition step, cluster spin coating + dev equipment. The developer consumables are in the deposition step.

- The 6µm copper lines are electroplated.

© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

WL-CSP Wafer Cost

	Scenario 1 Higher cost		Scenario 2 Lower cost	
	Cost	Breakdown	Cost	Breakdown
Depreciation Cost				
Manufacturing Cost				
Labor Cost				
STEPS COST				
Die cost				
Yield Losses				
TOTAL				
Manufacturing yield				



- The main part of the wafer cost is due to the Manufacturing Cost: between xx% and xx% of the cost.
- The yield losses is a major cost factor.
- The depreciation cost is between xx% and xx%.

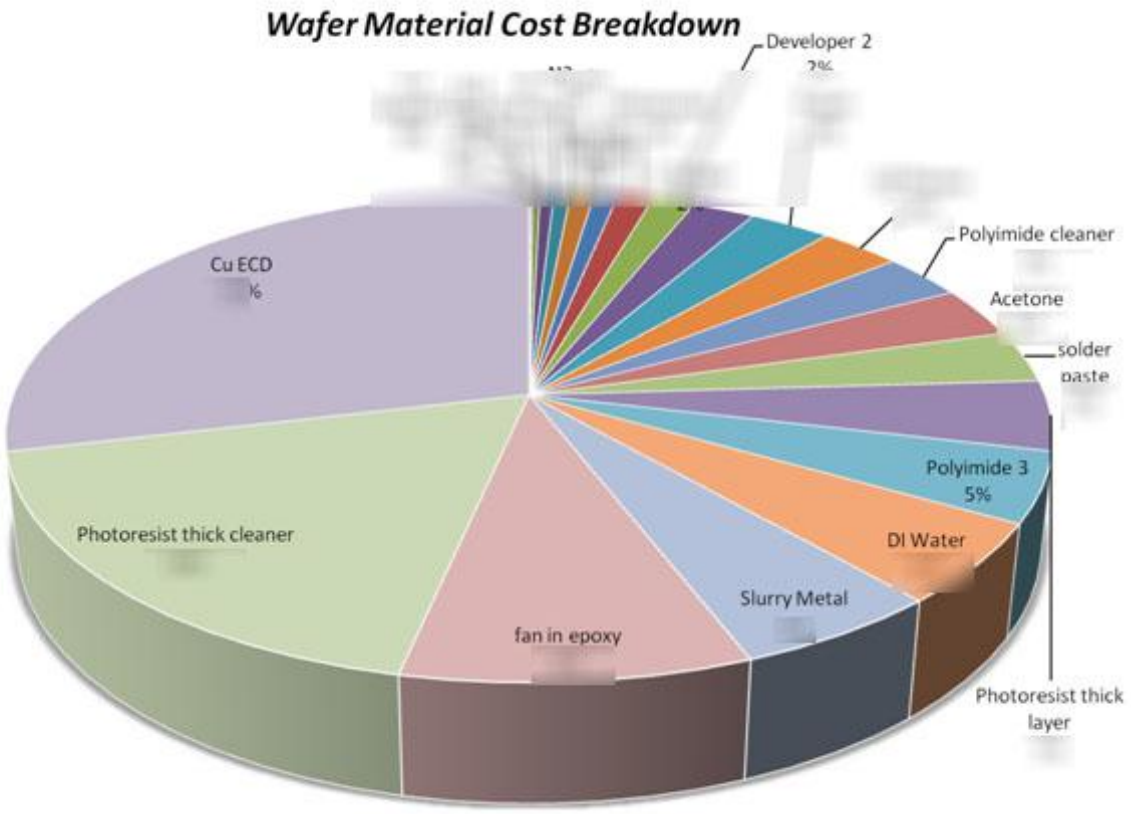
© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.

Wafer Cost per consumable family

Wafer cost per Consumable Family.

Material Name	Material Cost	Breakdown
SF6		
Cu Target		
CF4		
Al Etchant		
AP-309		
N2		
Photoresist		
Developer		
Ti Target		
Power		
O2 Plasma		
Polyimide cleaner		
Acetone		
solder paste		
Photoresist thick layer		
Polyimide		
DI Water		
Slurry Metal		
fan in epoxy		
Photoresist thick cleaner		
Cu ECD		
TOTAL		

- The cleaner used to etch the thick resin is expensive.
- Details of the material cost per step are given in the Excel spreadsheet.



Wafer cost per Material Family

© 2010 by SYSTEM PLUS CONSULTING, all rights reserved.