EWLP 309-pin by Casio Micronics – Fujitsu

The largest Full Wafer Level Chip Scale Package

Reverse costing analysis by System Plus Consulting

Reverse Analysis Report of the largest size Fan-In Wafer Level Package, featuring 309 pins with a pitch of 0.4mm !

System Plus Consulting is proud to publish the reverse costing report of one of the latest **Wafer Level Chip Scale Package** based on Casio Micronics' EWLP technology and used by Fujitsu for device MB39C311A, a Power Management Unit + Audio Interface Unit IC for mobile phone.

EWLP is an advanced technology for WL-CSP. All the packaging operations are done at the wafer level. The ball pitch is only 0.4mm and only one redistribution layer is used for the 309 balls of this 7.45x7.45 mm package. This WL-CSP is manufactured on 200mm wafers by Casio Micronics.

This report provides a complete teardown of the Casio Micronics/Fujitsu 0.4mm pitch WL-CSP package including:

- Detailed photos
- Material analysis
- Manufacturing Process Flow
- In-depth economical analysis
- Manufacturing cost breakdown
- Selling price estimation

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