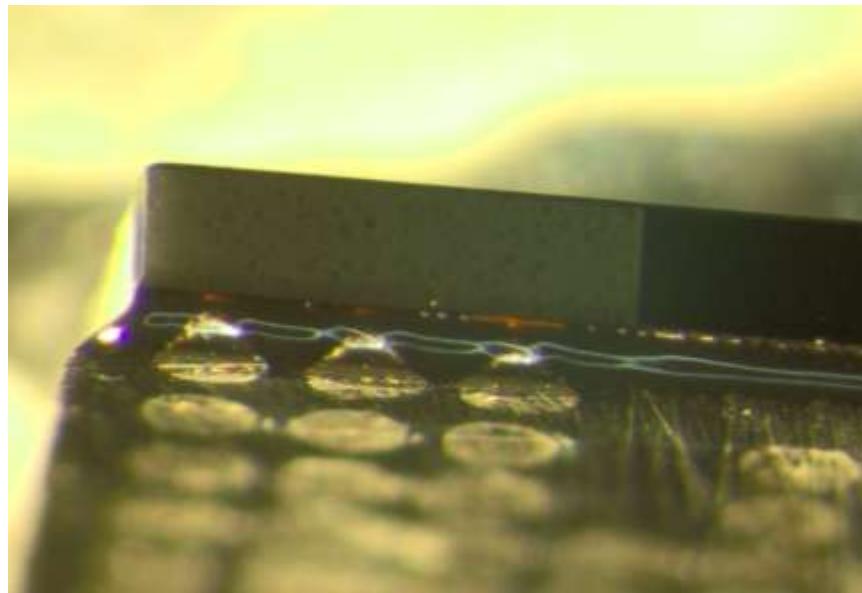


Reverse Costing analysis



eWLB (X-GOLD™ 213) by Infineon

Reverse analysis report of a Fan-out Wafer Level Package

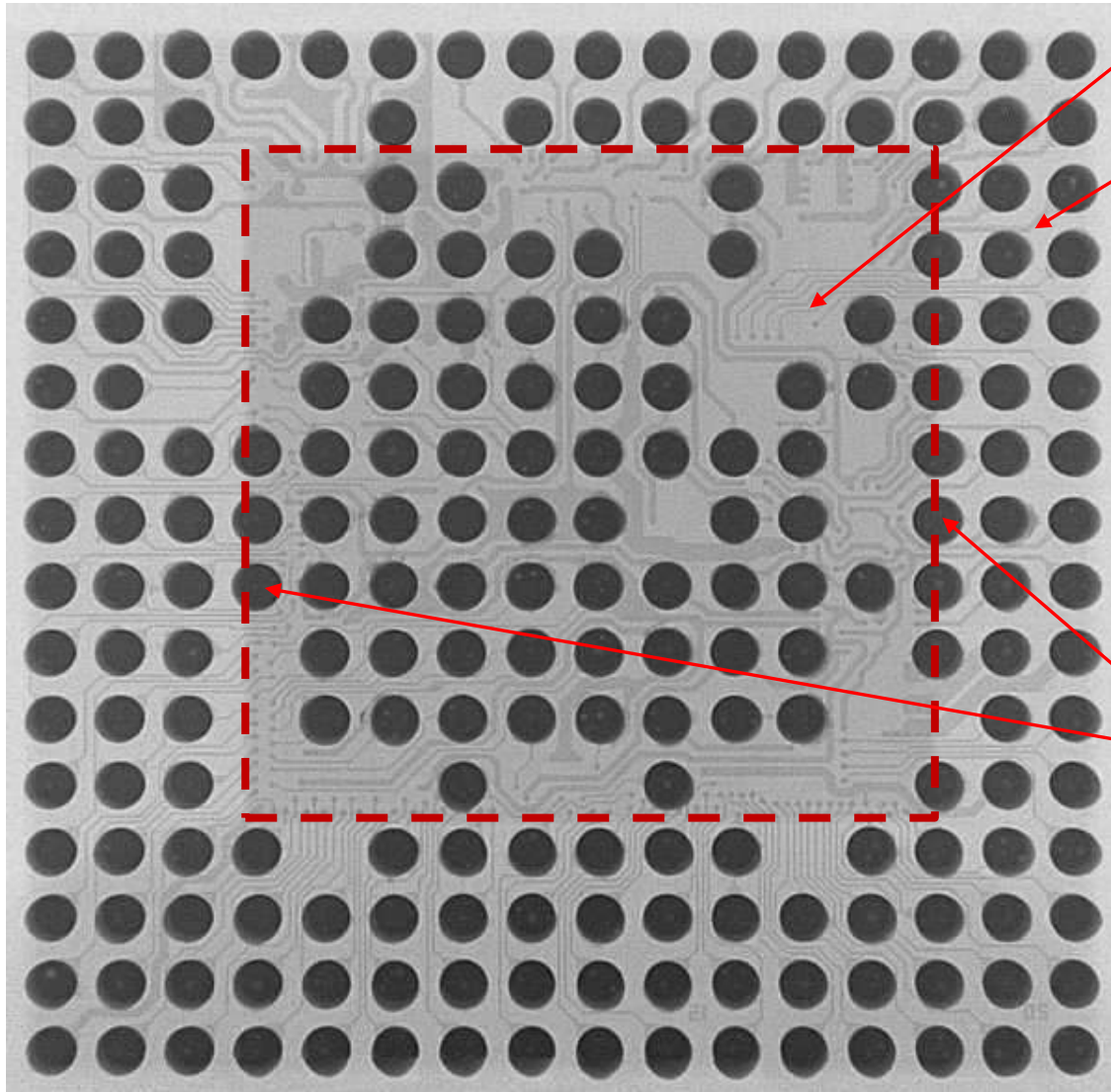
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This X-Ray picture of eWLB was taken after removal of the PCB.



Die
5.1mm x 5.1mm = 26.1mm²

Package
8mm x 8mm = 64mm²

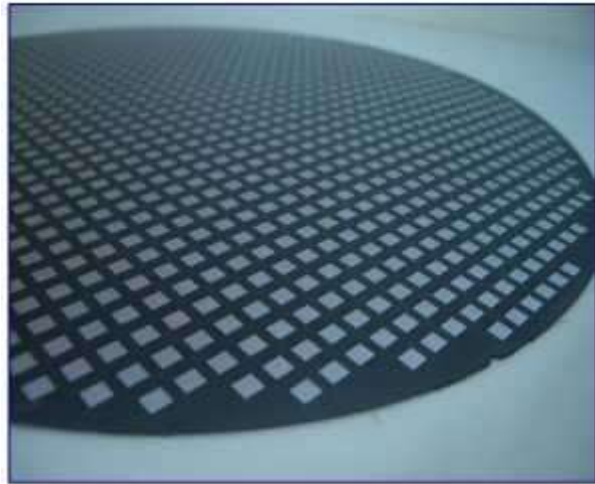
The fan-out ratio is 2.46
(package size over chip size)

The die is not centered in the package.

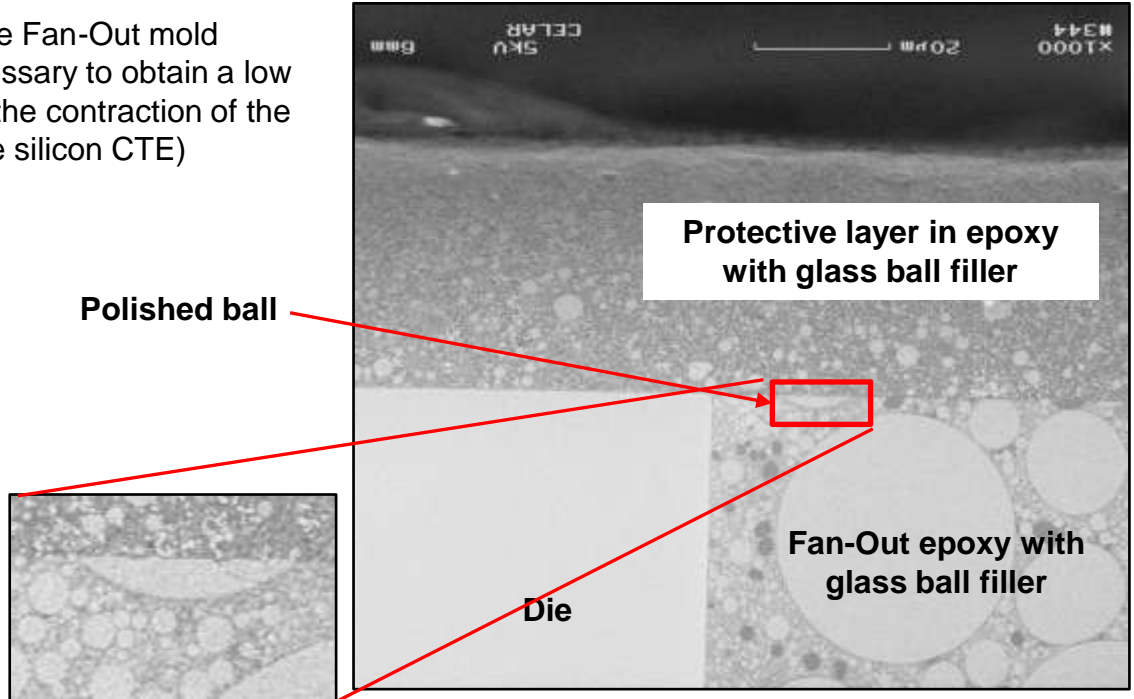
Some balls are right below the edge of the die and the fan-out area

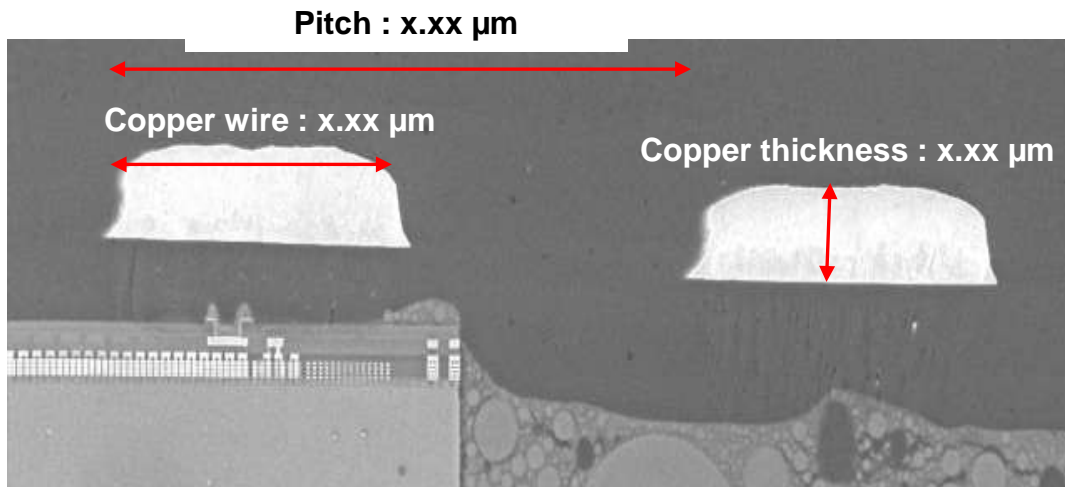
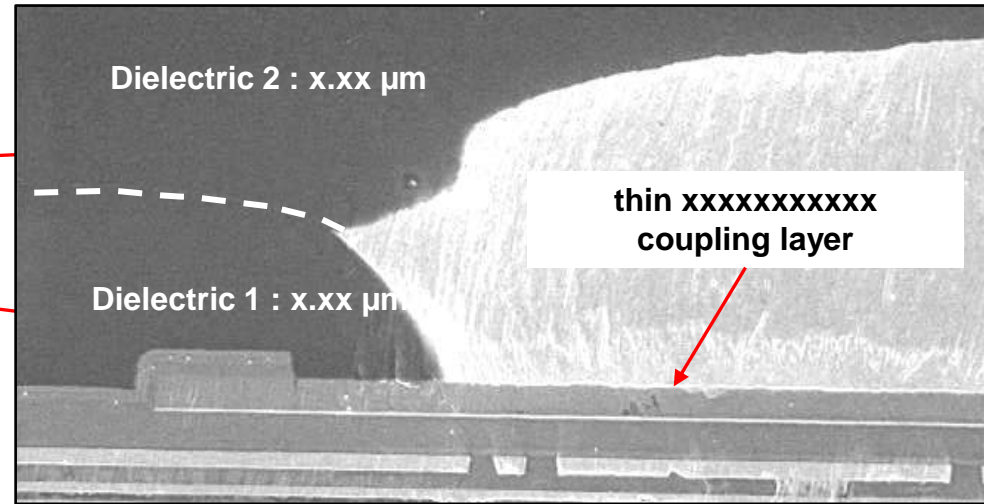
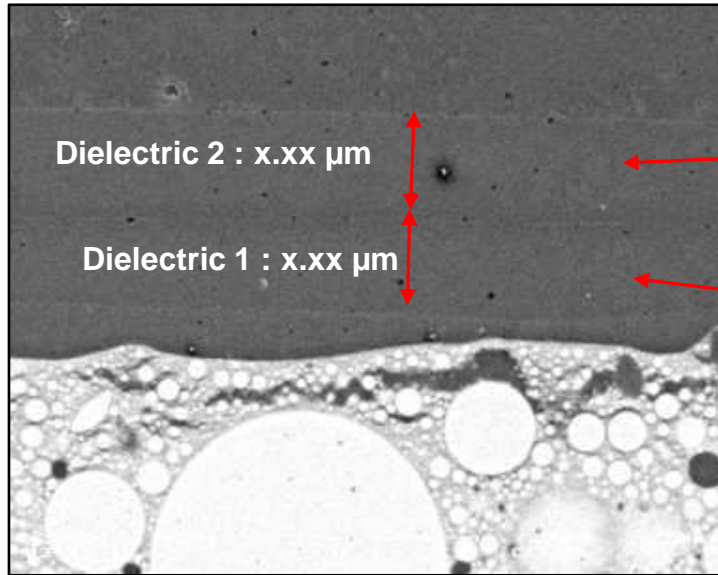
The back side of the wafer, after the wafer molding step, is grinded. It can be seen that the glass balls sealed within the mold compound were polished. A protective layer was deposited.

The filler content ratio is estimated at 75% of the Fan-Out mold compound. The high percentage of filler is necessary to obtain a low coefficient of thermal expansion (useful to limit the contraction of the reconfigured wafer at molding, and to match the silicon CTE)



Infineon doc : wafer redistributed



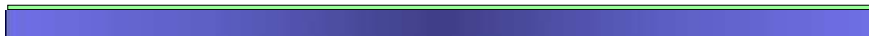


We estimate at x.xx ml the necessary volume of dielectric for each layer per 8" wafer.

1) Wafer preparation: wafer thinning and sawing



2) Lamination of foil onto carrier



3) Pick, flip and placement of known good tested IC's on foil



4) Wafer molding



5) Grinding of the epoxy resin (to release the stress difference between both sides so as to avoid wafer warping?)



6) spin-on deposition of a back-side epoxy resin protection layer



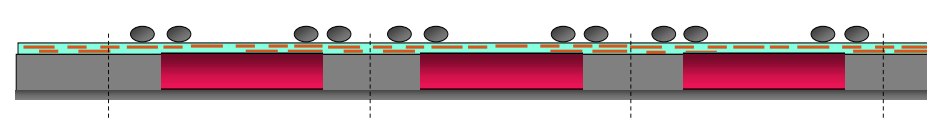
7) de-bonding and foil removal, wafer is turned upside down, plasma cleaning and planarization of the front side



8) Application of a redistribution layer (1 seed layer deposition, 2 dielectric layers, 1 copper layer)



9) Balling and singulation



Courtesy of



Fan Out WLP

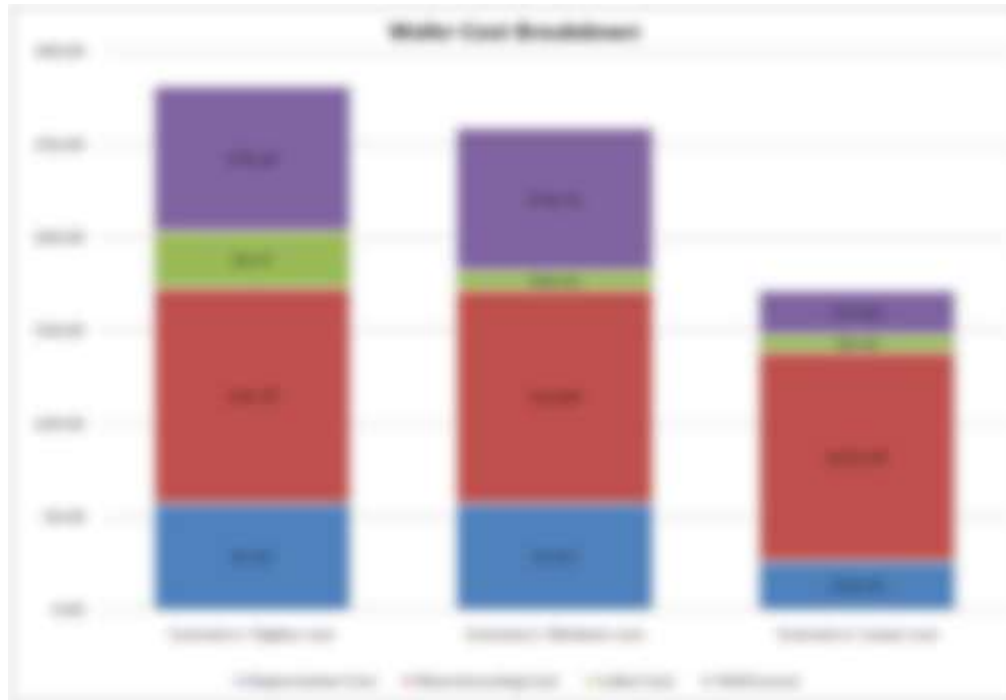
- ✦ Cleaning
- ✦ Adhesive film coating
- ✦ Pick and Place
- ✦ Fan-out molding
- ✦ Lateral grinding
- ✦ Fan-out grinding
- ✦ Cleaning
- ✦ Die Fixing
- ✦ Temporary bonding
- ✦ Cleaning
- ✦ Electrode (E-pad) coating
- ✦ Cleaning
- ✦ Test

- The carrier wafer is cleaned.
- An adhesive film is laminated onto the surface.

- The die is placed on the carrier wafer.
- The carrier wafer is mounted on a special carrier. It is connected with the equipment with flexible, movable lines.
- The carrier wafer is mounted on the carrier wafer.
- The top side of the carrier wafer is ground to allow for support. The carrier wafer is ground to allow for support.
- The carrier wafer is mounted on the carrier wafer.
- The carrier wafer is temporarily bonded to increase the rigidity. This step is optional. It is connected with the carrier wafer to increase the rigidity.
- It depends on the carrier wafer and the carrier wafer thickness.
- Some measurements are performed during the test step.

	Scenario 1 Higher cost		Scenario 2 Medium cost		Scenario 3 Lower cost	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Depreciation Cost	10.00	10.00%	10.00	10.00%	10.00	10.00%
Manufacturing Cost	10.00	10.00%	10.00	10.00%	10.00	10.00%
Labor Cost	10.00	10.00%	10.00	10.00%	10.00	10.00%
STEPS COST	30.00	100%	30.00	100%	30.00	100%
Die cost	10.00	10.00%	10.00	10.00%	10.00	10.00%
Yield Losses	10.00	10.00%	10.00	10.00%	10.00	10.00%
TOTAL	50.00	100%	50.00	100%	50.00	100%
Manufacturing yield	90%		90%		90%	

Wafer cost breakdown



- The main part of the wafer cost is due to the Manufacturing Cost: xx% in the “medium cost” version.
- The yield losses is a major cost factor, up to xx% for the “low yield” versions.
- The depreciation cost around xx% if new equipments are used (Scenarios 1 and 2).
- The labor cost is much higher in Germany (Sc. 1) but the overall weight is only xx%.