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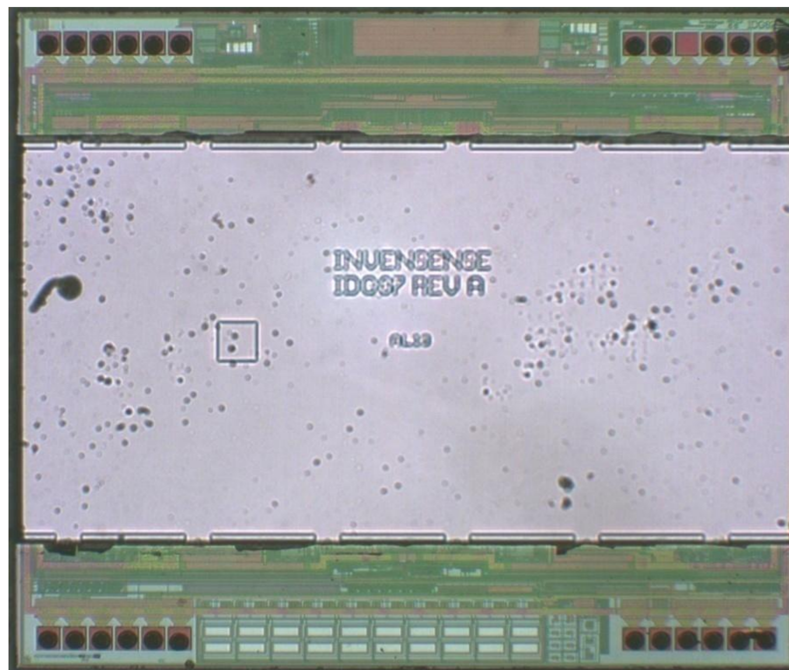
Reverse Costing analysis



InvenSense IDG-600/650
Dual-Axis MEMS Gyroscope

January 2010 - Version 1

Written by: Romain FRAUX

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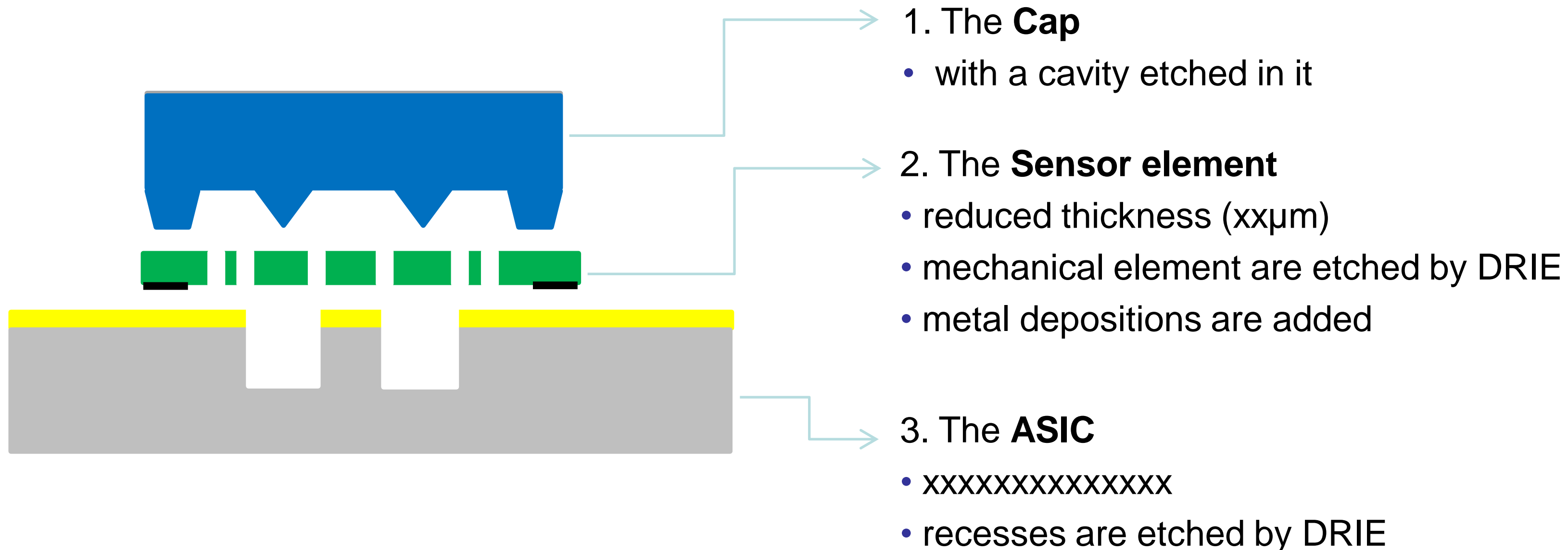
Executive Summary

- 3 wafers are used to build the IDG-600/650 component and bonded together



- The sensing elements are made in a thin silicon substrate and are protected by a silicon cap.
- The ASIC wafer is etched (deep recesses) to let the sensing elements free, and then bonded with the MEMS + Cap compound.
- The ASIC is using a xxxxx process
- The sensor is protected and thus can be packaged using a standard assembly process.

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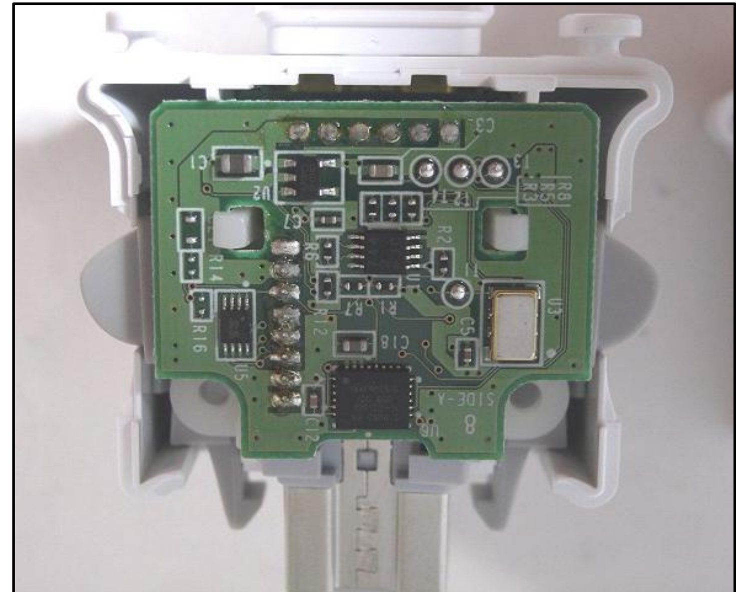
InvenSense Profile

- **IDG-600/650 products:**
  - ✓ **IDG-600 : Included in the Nintendo Wii Motion Plus accessory**
  - ✓ **IDG-650 : standard component**



IDG-600 and IDG-650 are exactly similar

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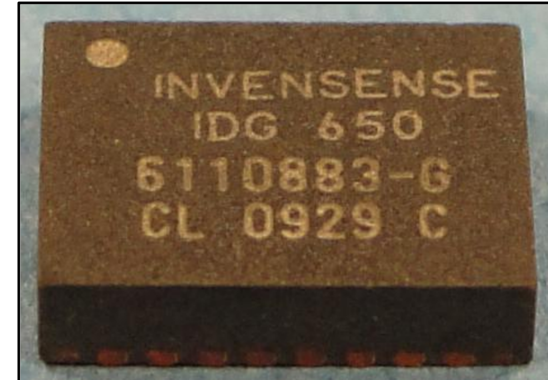
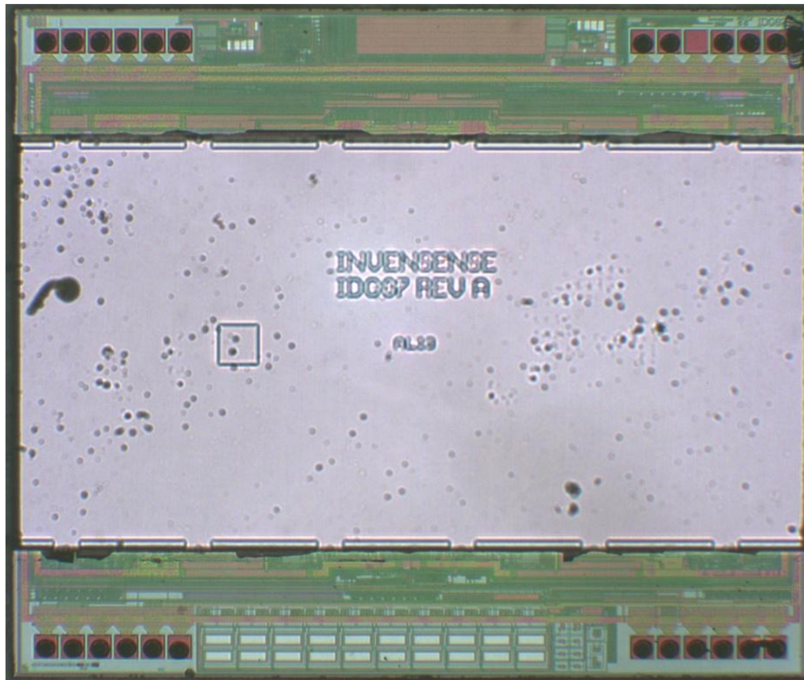
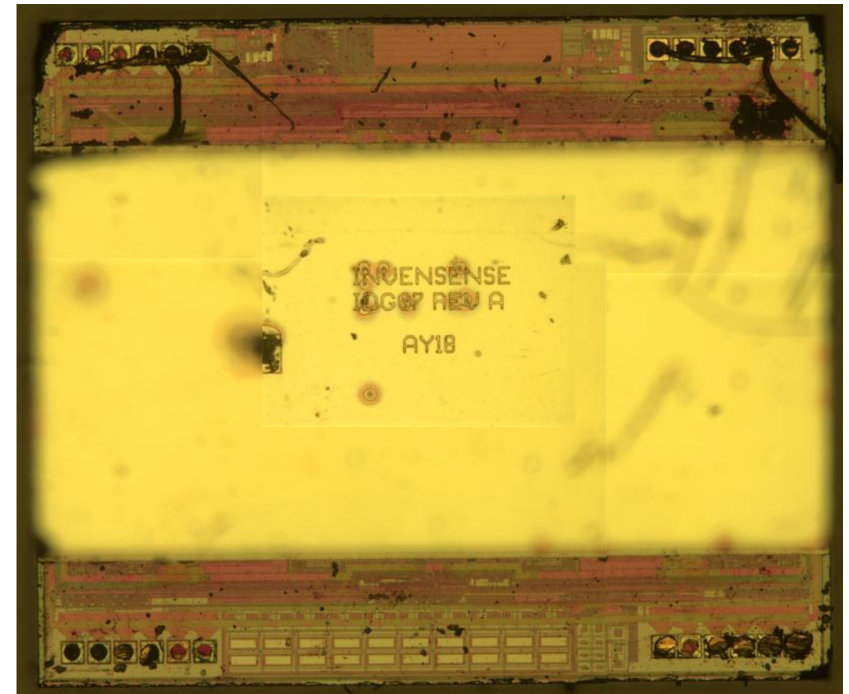
IDG-600 / IDG-650 Comparison

- **IDG-600/650 products (Dies comparison):**







IDG-600 and IDG-650 share exactly the same dies

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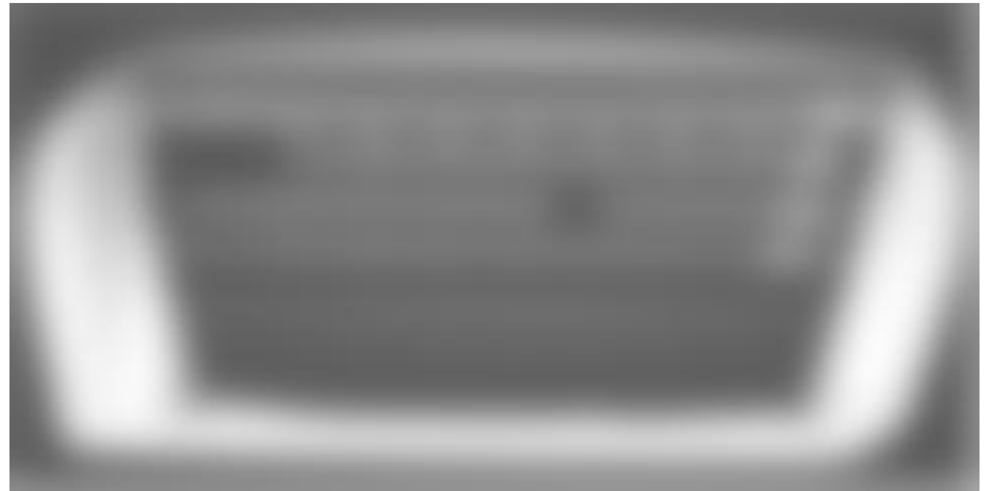
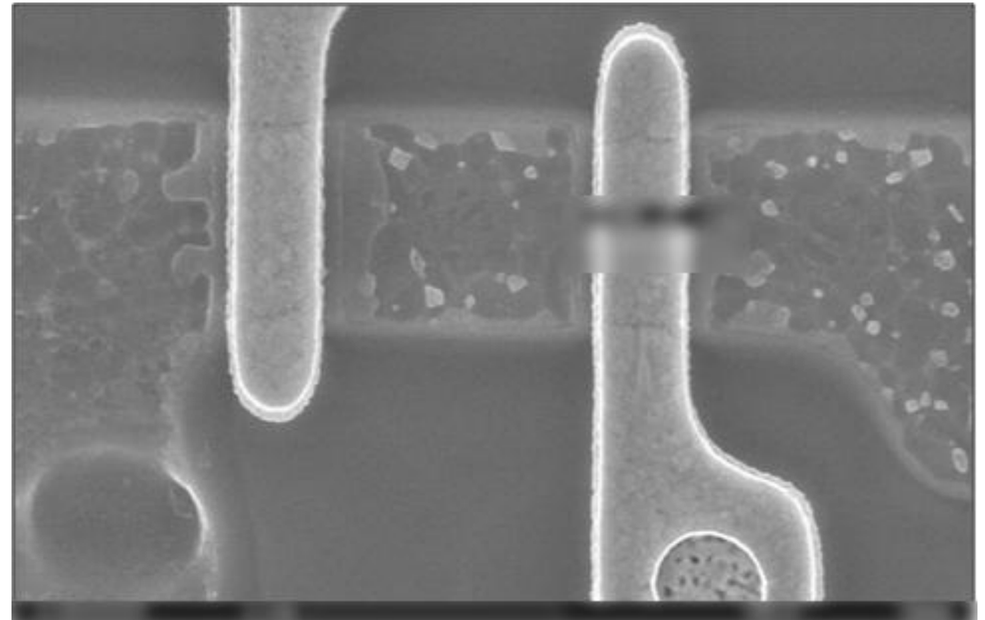
ASIC minimal dimensions and metal layers

- **Number of metal layers :**
  - ✓ **xx Aluminum planar**

- **Minimal dimension in circuit :**
  - ✓**xxµm**



SEM image of the xx Aluminum Metal Layer (FIB cut)



Transistor Gate Length in Logic area

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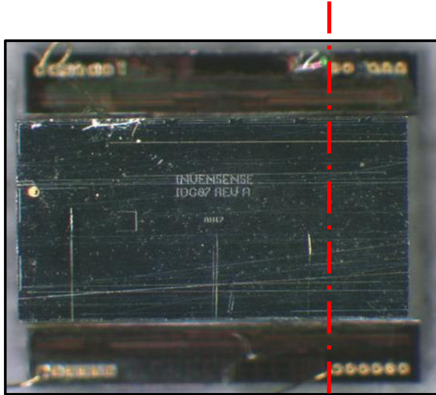
Component Cross-Section



Cross-Sectional Plane

Cap

Sensor

ASIC

Component Cross-Section

Cap thickness: xxµm

Sensor thickness: xxµm

ASIC thickness: xxµm

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MEMS Process Flow 2/3 (Sensor)

• The sensor wafer is manufactured in the same fab that the cap wafer:

- Substrate:
- Process type:
- Metal layers:
- Special Steps:
- Lithography steps:

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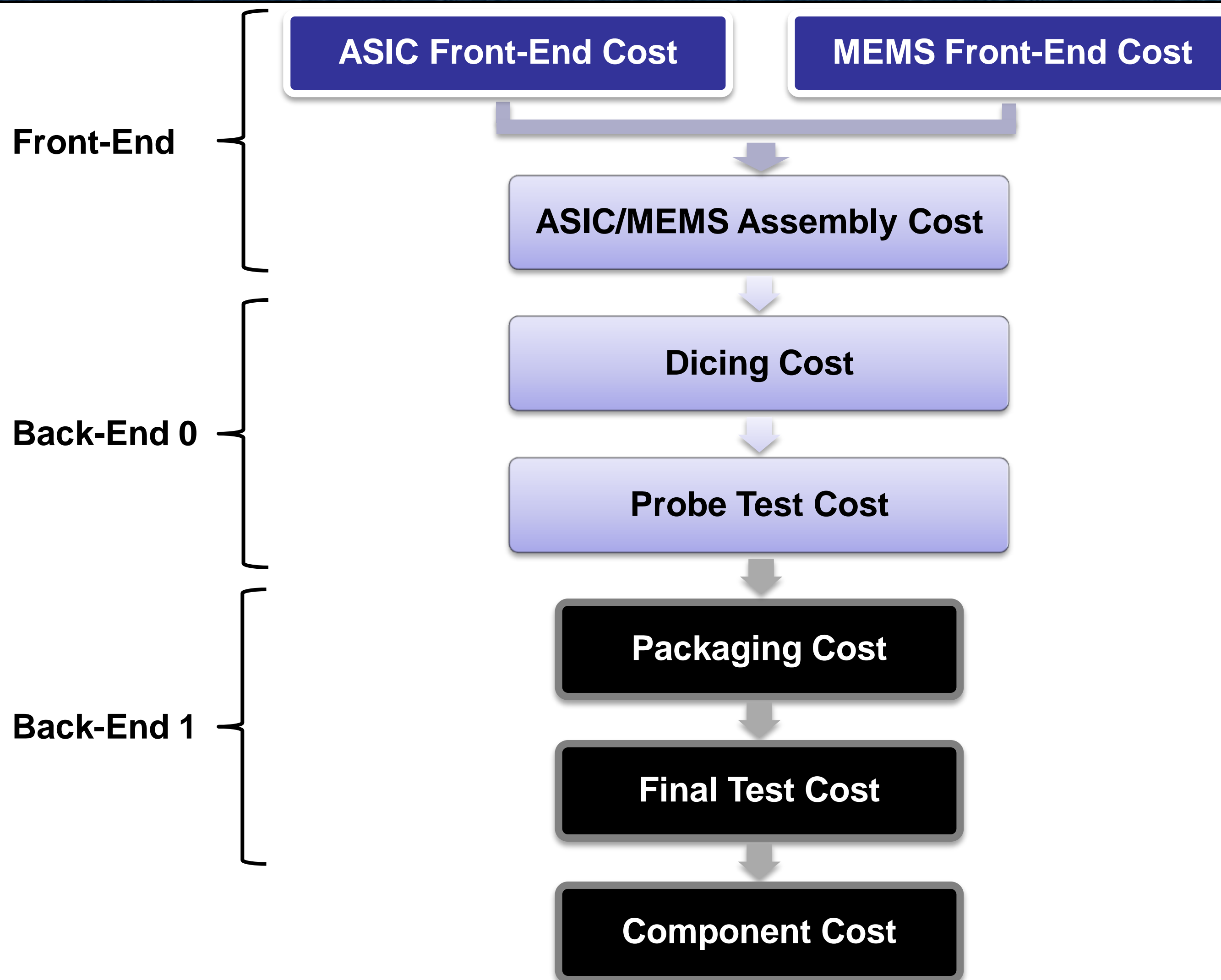
Main steps of economic analysis



- **We perform the economic analysis of the ASIC with the IC Purchaser software.**
- **We perform the economic analysis of the MEMS and the packaging with the MEMS CoSim+ software.**

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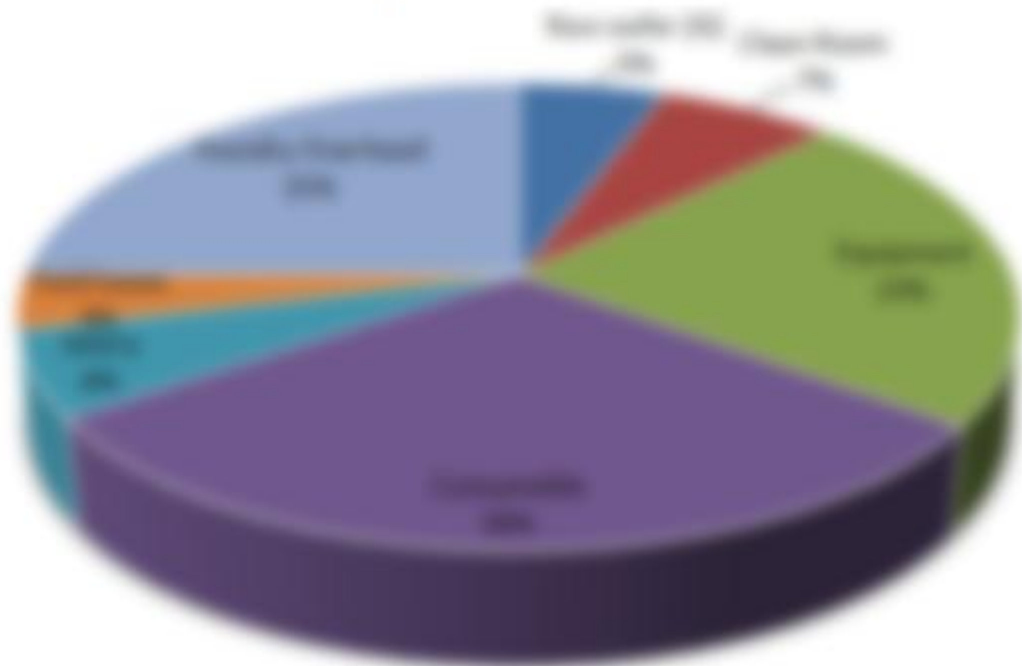
ASIC Front-End Cost (CMOS Manufacturing)

ASIC CMOS Manufacturing (CMOS Foundry)	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw wafer (Si)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Clean Room	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Equipment	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Consumable	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Salary	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Foundry Overhead	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
CMOS Manufacturing Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

ASIC CMOS Manufacturing Cost Breakdown (Medium Yield)



- **The ASIC CMOS Manufacturing cost range from $xx to $xx according to yield variations.**
- **By adding the foundry overhead of xxx, the cost range from $xx to $xx.**
- **The main part of the wafer cost is due to the xxx with xx%.**
- **The manufacturing yield ranges from xx% to xx%.**

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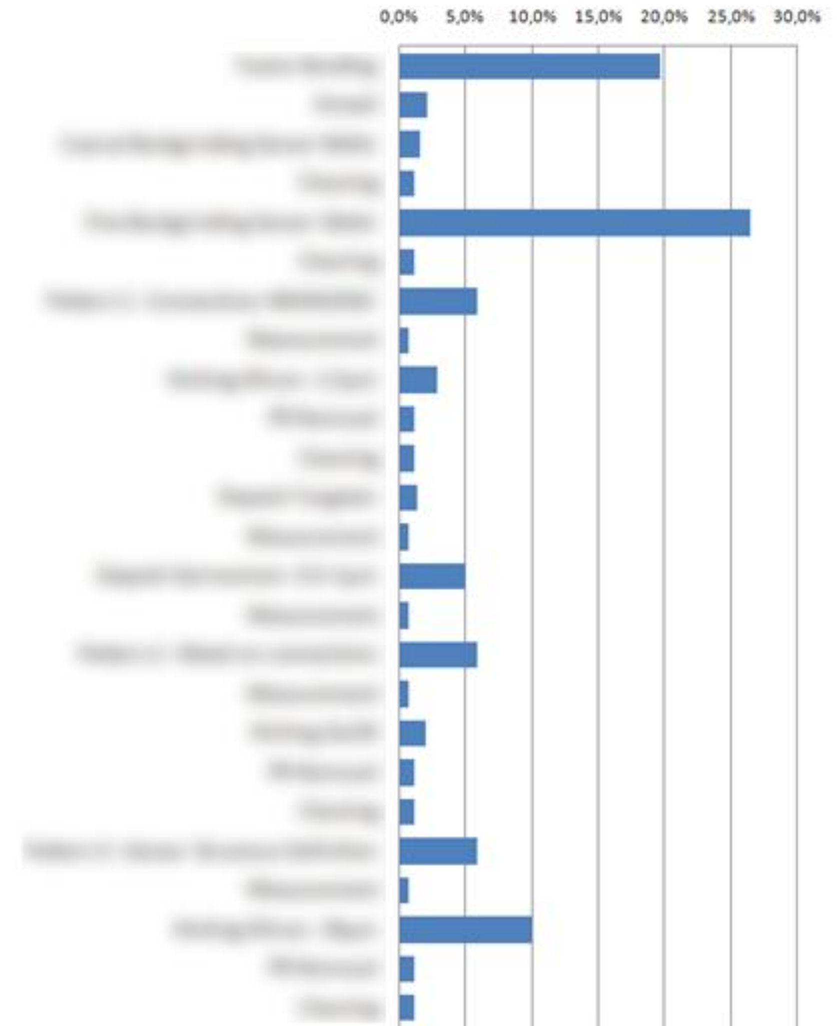
MEMS Front-End Cost per Process Steps 2/2

Sensor Wafer	Cost	Breakdown
[illegible]	[illegible]	19,6%
[illegible]	[illegible]	2,1%
[illegible]	[illegible]	1,5%
[illegible]	[illegible]	1,1%
[illegible]	[illegible]	26,5%
[illegible]	[illegible]	1,1%
[illegible]	[illegible]	5,8%
[illegible]	[illegible]	0,6%
[illegible]	[illegible]	2,8%
[illegible]	[illegible]	1,0%
[illegible]	[illegible]	1,1%
[illegible]	[illegible]	1,3%
[illegible]	[illegible]	0,6%
[illegible]	[illegible]	5,0%
[illegible]	[illegible]	0,6%
[illegible]	[illegible]	5,8%
[illegible]	[illegible]	0,6%
[illegible]	[illegible]	1,9%
[illegible]	[illegible]	1,0%
[illegible]	[illegible]	1,1%
[illegible]	[illegible]	5,8%
[illegible]	[illegible]	0,6%
[illegible]	[illegible]	10,0%
[illegible]	[illegible]	1,0%
[illegible]	[illegible]	1,1%
TOTAL	[illegible]	

Sensor Manufacturing Step Cost Breakdown



Sensor Manufacturing Steps Cost
(Simulated with MEMS CoSim+ Cost Simulation Tool)

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Die Cost

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
FE : ASIC Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : CAP + Sensor Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
FE : ASIC/MEMS Assembly Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Probe Test + Dicing Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 : Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MEMS Foundry Overhead Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Die Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Die Cost Breakdown (Medium Yields)

- **The final die cost range from $xx to $xx according to yield variations.**
- **The back-end 0 cost (probe test and dicing) represent xx% of the cost of the die.**
- **The yield losses costs due to probe and dicing represent xx% of the total manufacturing cost.**
  - **The die cost includes the rejects at probe test and dicing.**
  - **The yield losses represents the bad dies out for the garbage.**

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