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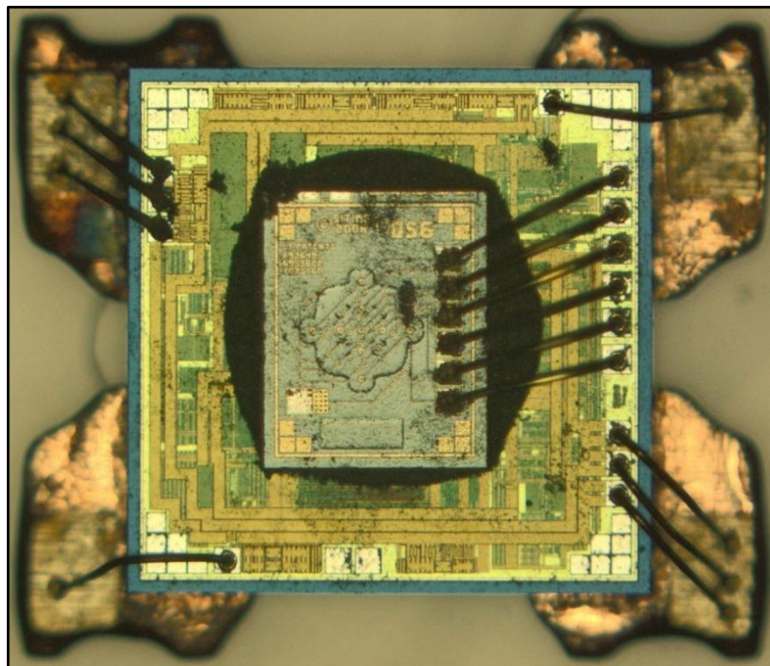
Reverse Costing analysis



SiTime SiT8002 MEMS Oscillator

December 2009 - Version 1

Written by: Romain FRAUX

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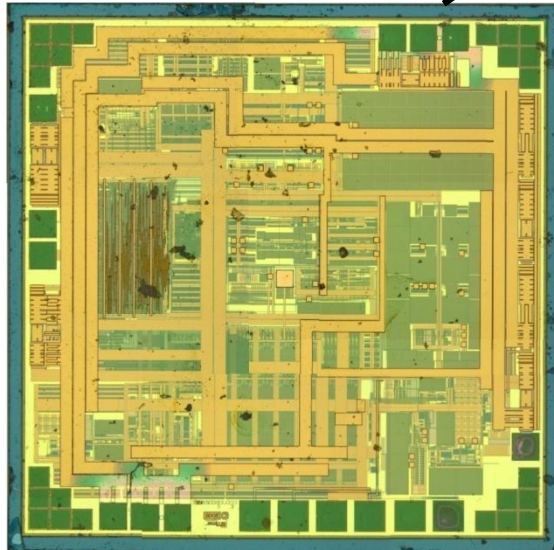
Executive Summary

SiT8002

Assembly in package
Encapsulation
Final test

ASIC



CMOS process
x.xxµm, x metallization layers, x polysilicon Layers
xx Lithography steps

MEMS Resonator

SOI Substrate
Sealed with EpiSeal™ Process
xx Lithography steps

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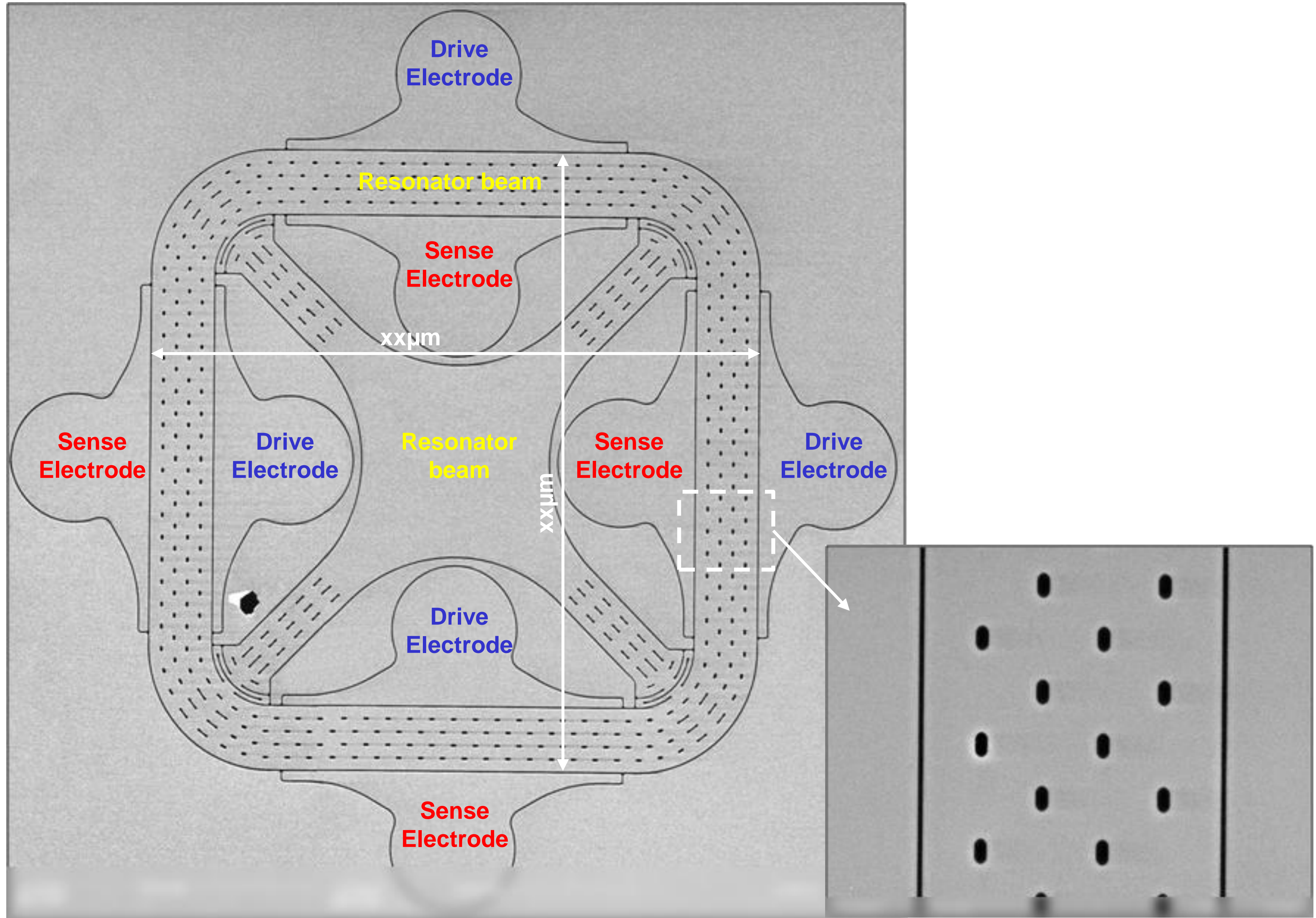
Resonator Details



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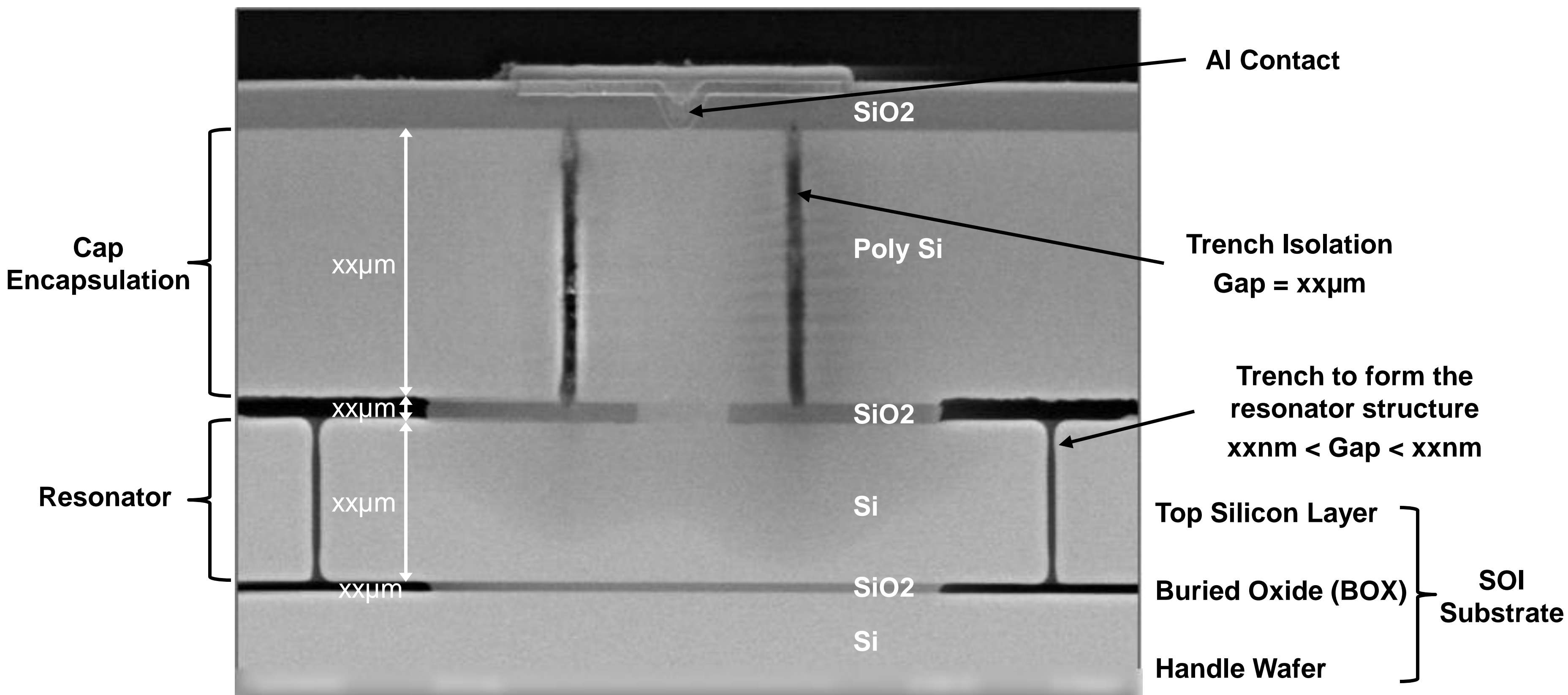
Resonator Cross-Section



MEMS Cross section

A **Bonded SOI wafer** is used to realize the **xxµm top Silicon layer**. The resonator structure is formed in the top silicon layer by **DRIE**. An **oxide sacrificial layer (xxµm)** is deposited by LPCVD on the silicon resonator.

The **xxµm of polysilicon** is deposited in an epitaxial reactor and is used to seal the resonator. Trench isolation are made in the polysilicon layer by **DRIE**.

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MEMS Process Flow 2/2

- **The MEMS is manufactured by xxxx in the 200mm xxxx foundry:**
  - **Process type:**
  - **Metal layers:**
  - **Polysilicon layer:**
  - **Lithography steps:**

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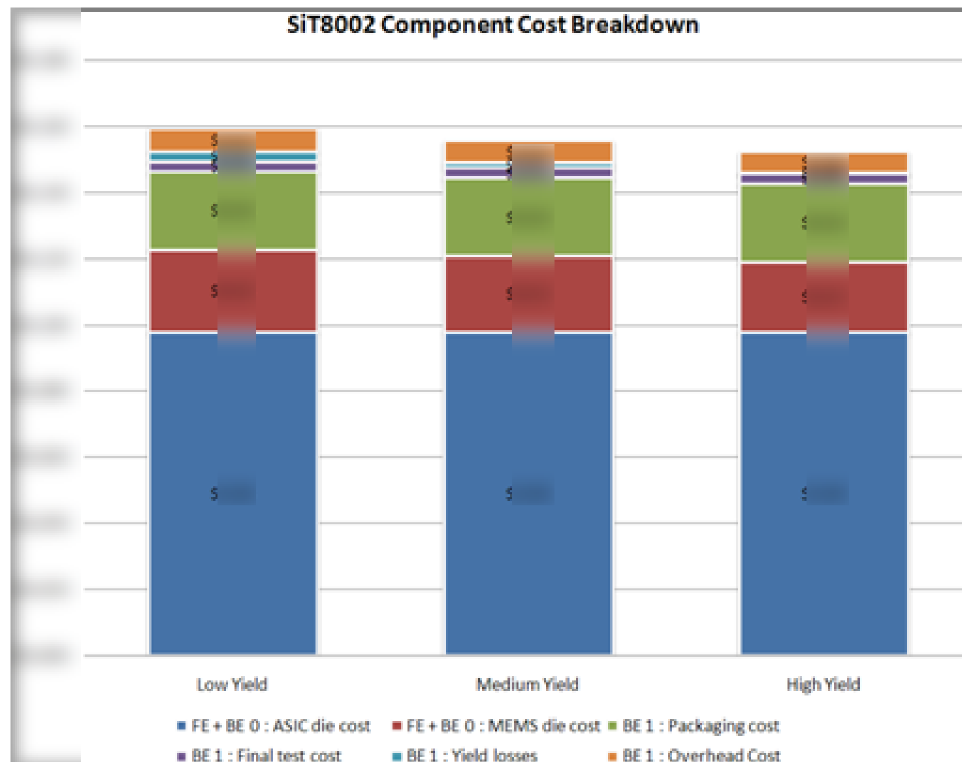
Synthesis of the cost analysis

- The SiT8002 component is designed by SiTime Corporation.
- The production of the ASIC by xxx is assumed to take place in the 200mm xxx wafer foundry in xxx.
  - ➢ The ASIC wafer cost is estimated at $xxx, the die cost is estimated at $xxx
- The production of the MEMS by xxx is assumed to take place in the 200mm xxx fab in xxx.
  - ➢ The MEMS wafer cost is estimated at $xxx, the die cost is estimated at $xxx.
- The packaging of the two dies by xxx is assumed to take place in xxx.
  - ➢ The packaging cost is estimated at $xxx.
- The component manufacturing cost range from $xxx to $xxx according to yield hypotheses.



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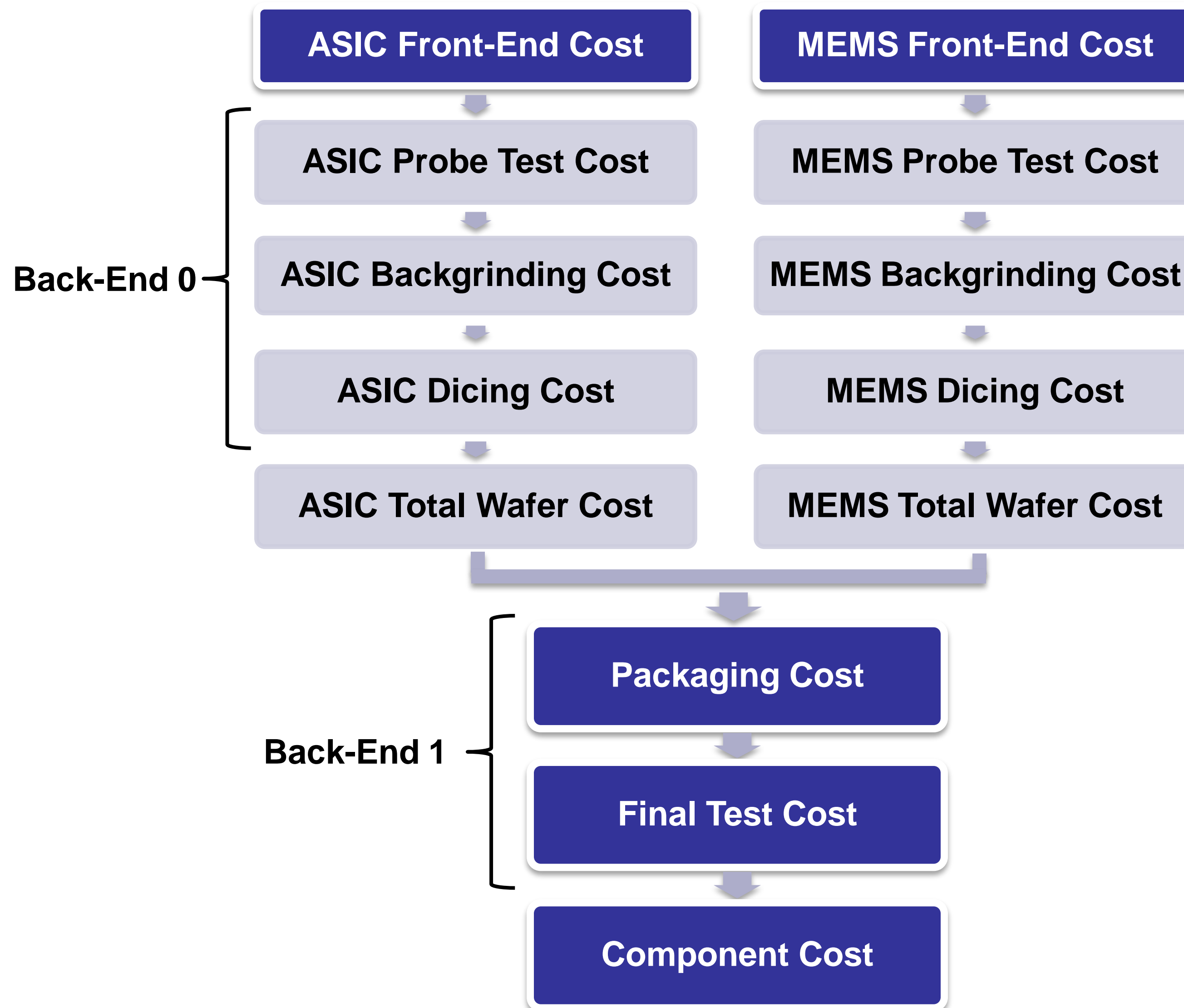
Main steps of economic analysis



- We perform the economic analysis of the ASIC with the IC Purchaser software.
- We perform the economic analysis of the MEMS and the packaging with the MEMS CoSim+ software.

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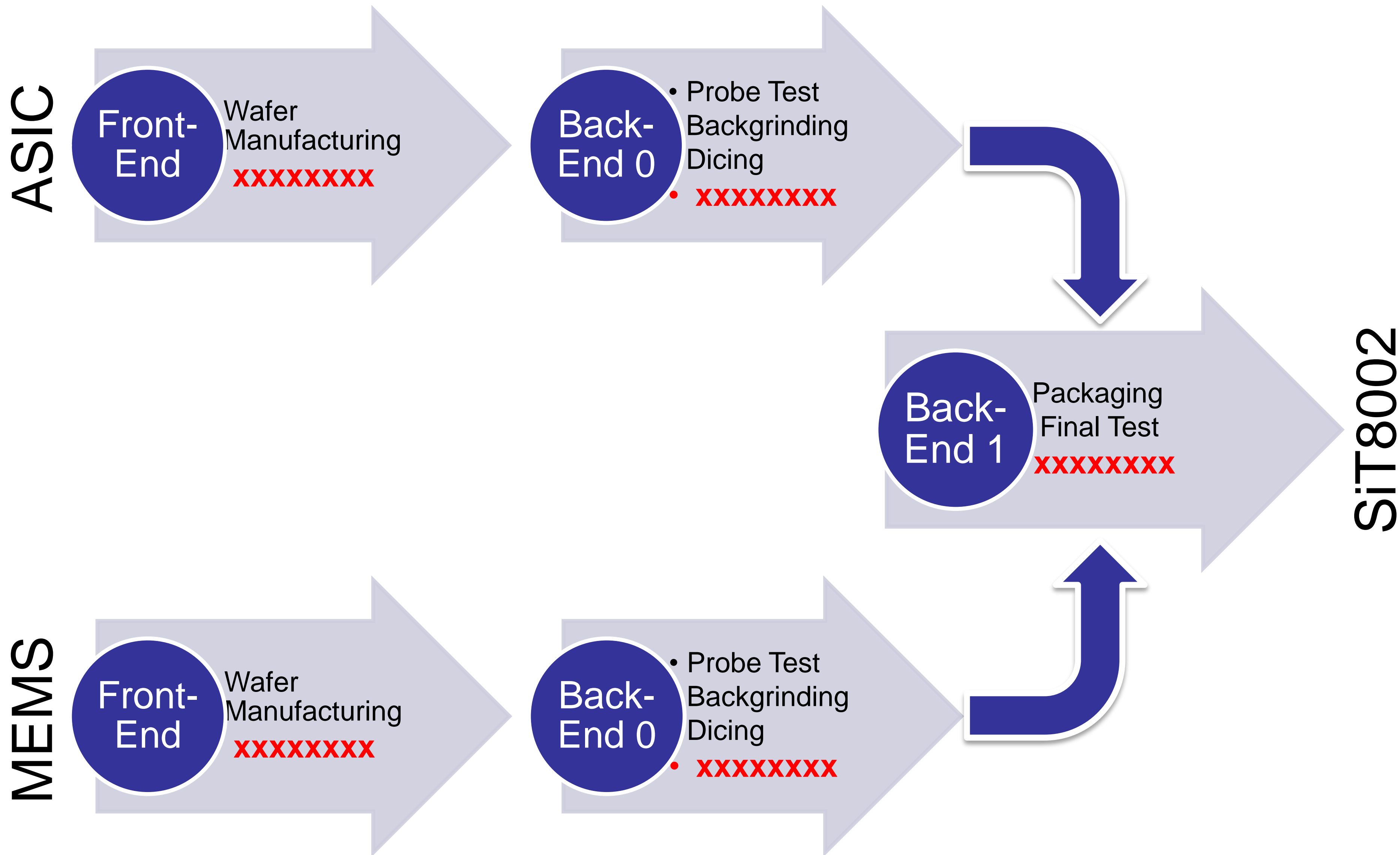
Supply Chain Analysis



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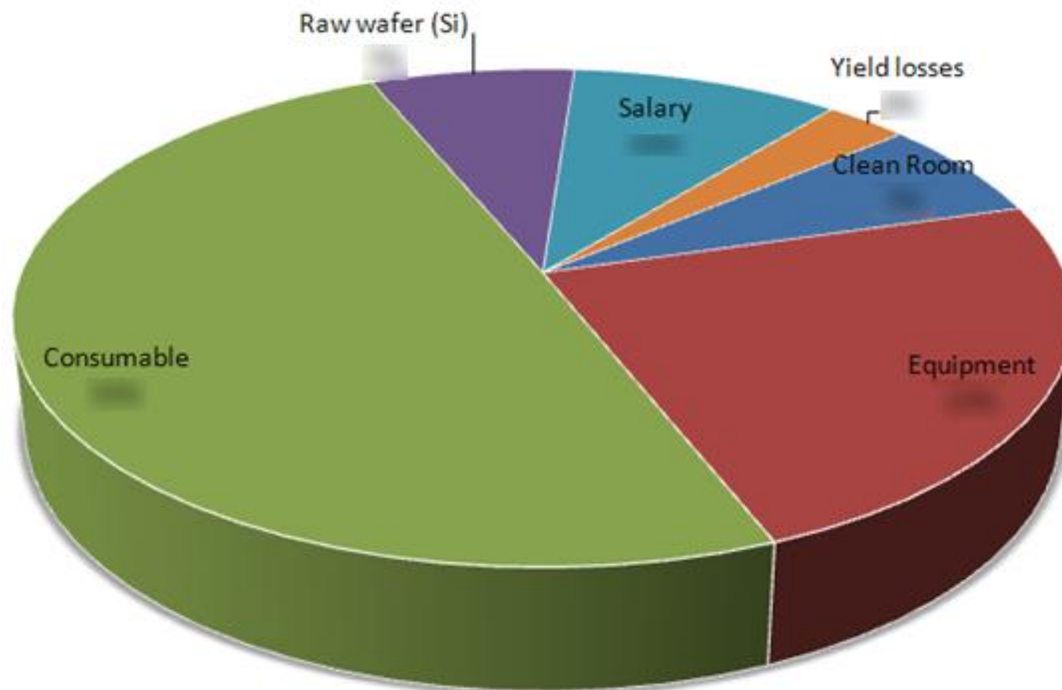
ASIC Front-End Cost

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Clean Room	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Equipment	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Consumable	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Raw wafer (Si)	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Salary	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Front-End Cost	[illegible]		[illegible]		[illegible]	
Cost with Foundry Overhead	[illegible]		[illegible]		[illegible]	



- Very low wafer cost decrease because the technology is mature.
- The main part of the wafer cost is due to the consumables with xx%. The salary part is xx%. This is an average value for production in xxx.
- The manufacturing yield ranges from xx% to xx%. The mature technology explains these values.

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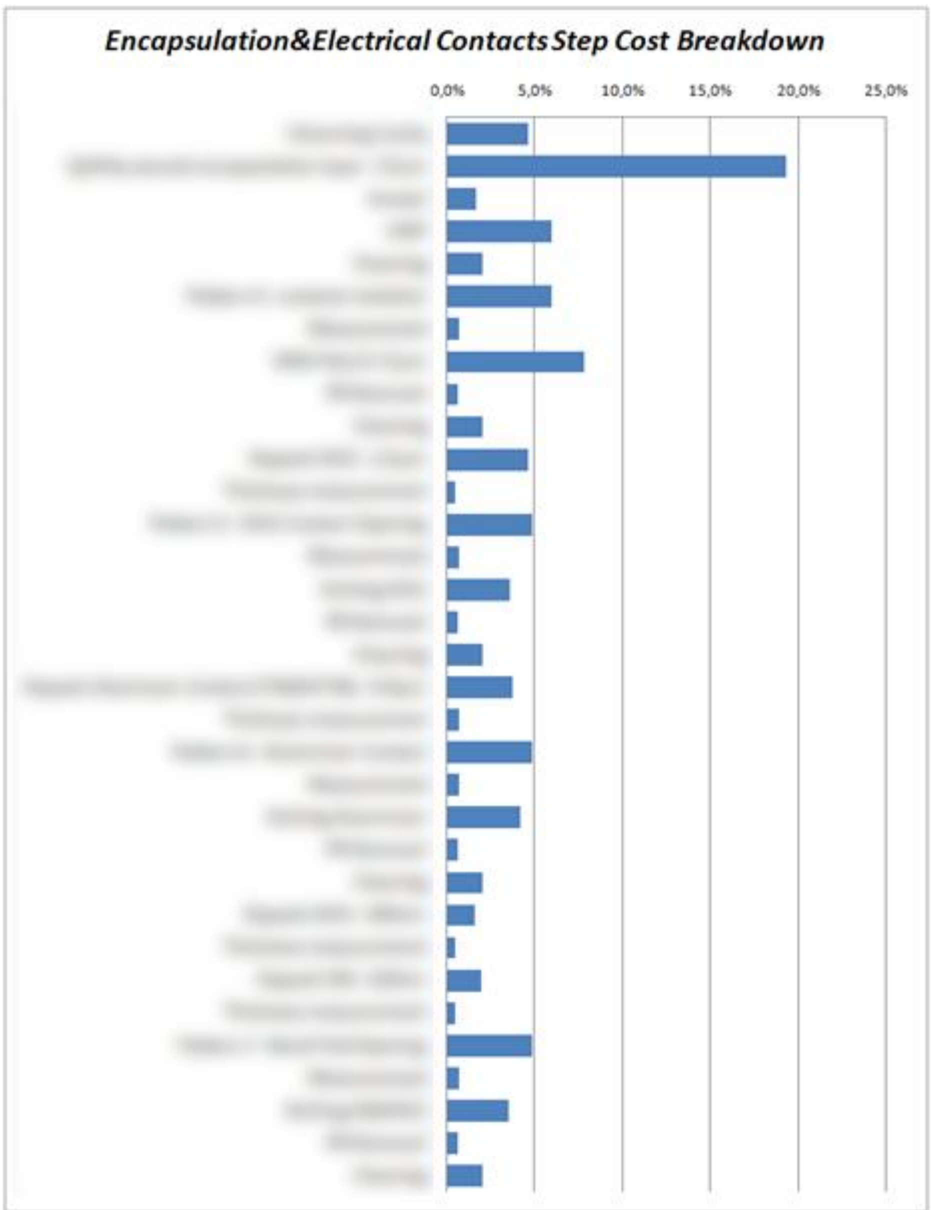
Front-End Cost Breakdown per Process Steps 2/2

Encapsulation & Electrical Contacts	Cost	Breakdown
[illegible]	$ [illegible]	4,6%
[illegible]	$ [illegible]	19,3%
[illegible]	$ [illegible]	1,7%
[illegible]	$ [illegible]	6,0%
[illegible]	$ [illegible]	2,0%
[illegible]	$ [illegible]	6,0%
[illegible]	$ [illegible]	0,7%
[illegible]	$ [illegible]	7,8%
[illegible]	$ [illegible]	0,6%
[illegible]	$ [illegible]	2,0%
[illegible]	$ [illegible]	4,6%
[illegible]	$ [illegible]	0,5%
[illegible]	$ [illegible]	4,9%
[illegible]	$ [illegible]	0,7%
[illegible]	$ [illegible]	3,6%
[illegible]	$ [illegible]	0,6%
[illegible]	$ [illegible]	2,0%
[illegible]	$ [illegible]	3,7%
[illegible]	$ [illegible]	0,7%
[illegible]	$ [illegible]	4,9%
[illegible]	$ [illegible]	0,7%
[illegible]	$ [illegible]	4,2%
[illegible]	$ [illegible]	0,6%
[illegible]	$ [illegible]	2,0%
[illegible]	$ [illegible]	1,6%
[illegible]	$ [illegible]	0,5%
[illegible]	$ [illegible]	1,9%
[illegible]	$ [illegible]	0,5%
[illegible]	$ [illegible]	4,9%
[illegible]	$ [illegible]	0,7%
[illegible]	$ [illegible]	3,5%
[illegible]	$ [illegible]	0,6%
[illegible]	$ [illegible]	2,0%
TOTAL	$ [illegible]	



Encapsulation Steps Cost

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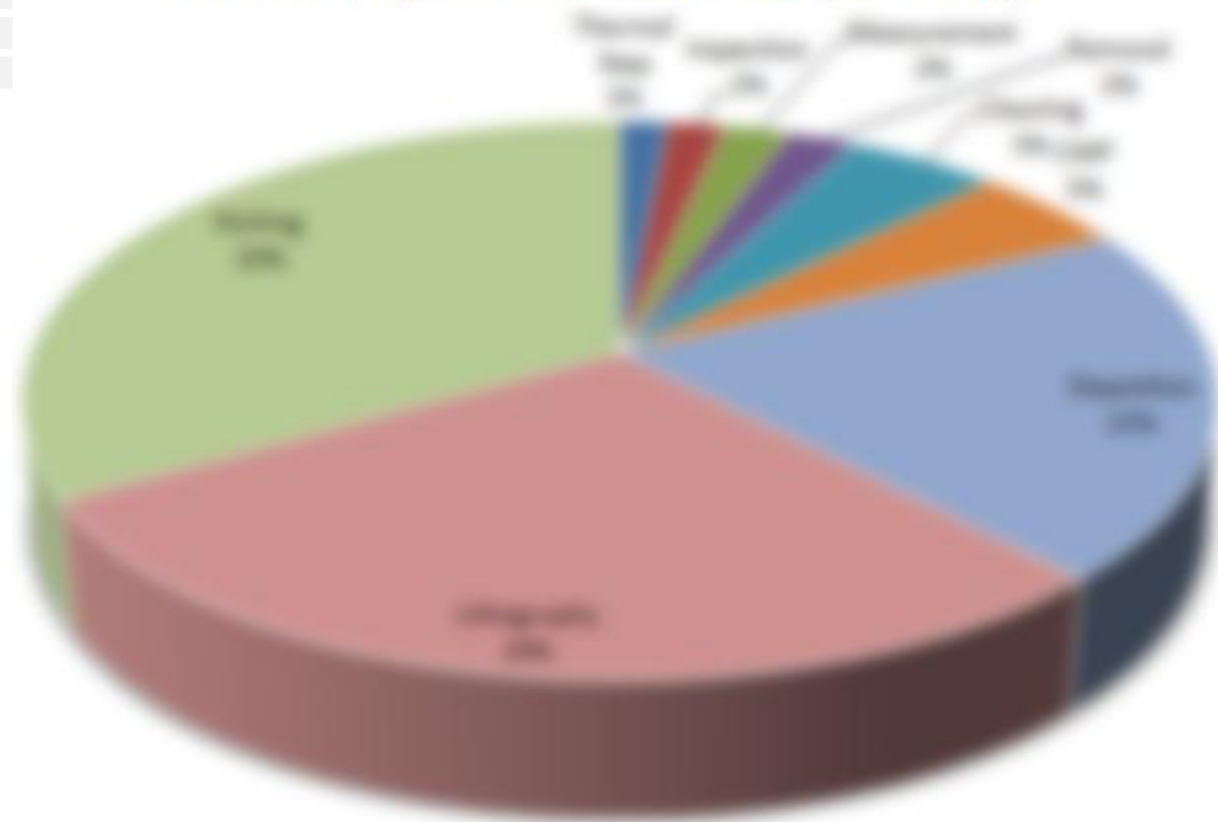
Front-End : Equipment Cost per Family

Equipment Family	Equipment Cost	Breakdown
Thermal Step	$[illegible]	[illegible]%
Inspection	$[illegible]	[illegible]%
Measurement	$[illegible]	[illegible]%
Removal	$[illegible]	[illegible]%
Cleaning	$[illegible]	[illegible]%
CMP	$[illegible]	[illegible]%
Deposition	$[illegible]	[illegible]%
Lithography	$[illegible]	[illegible]%
Etching	$[illegible]	[illegible]%
TOTAL	$[illegible]	

MEMS Equipment Cost per Family (Simulated with MEMS CoSim+ Cost Simulation Tool)

- **The main part of the equipment cost is due to the xxx steps (xx%). The xxxx explain this result.**

- **Details of the equipment cost per step are given in the Excel Spreadsheet.**



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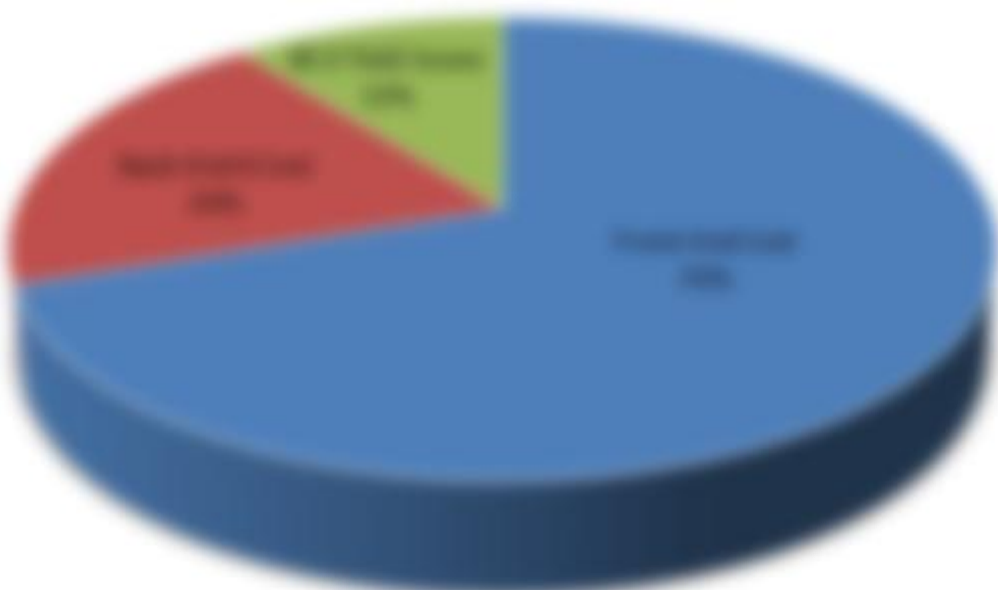
MEMS Die Cost

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Front-End Cost with Overhead	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Back-End 0 Cost with Overhead	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MEMS Wafer Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Nb of potential dies per wafer	[illegible]		[illegible]		[illegible]	
Nb of good dies per wafer	[illegible]		[illegible]		[illegible]	
Front-End Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Back-End 0 Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE 0 Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
MEMS Die Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

MEMS Die Cost Breakdown (Medium Yields)



- **The final MEMS die cost range from $xx to $xx according to yield variations.**
- **The back-end 0 cost (probe test, backgrinding and dicing) represent xx% of the cost of the die.**
- **The yield losses costs due to probe and dicing represent xx% of the total manufacturing cost.**
  - **The MEMS cost includes the rejects at probe test and dicing.**
  - **The yield losses represents the bad dies out for the garbage.**

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SiT8002 Packaging Hypothesis & Process Flow

- **Standard MLF (QFN type) package.**
  - ✓ **4-Lands**
  - ✓ **2.50 x 2.00 x 0.75mm**
- **2 dies to be assembled in the package**
  - ✓ **ASIC : xxmm²**
  - ✓ **MEMS : xxmm²**
  - ✓ **Stacked dies (conductive epoxy between the two dies)**
  - ✓ **8 bondings ASIC → Leadframe**
    - ➢ **Gold, xxµm diameter, ~1mm length**
  - ✓ **6 bondings MEMS → ASIC**
    - ➢ **Gold, xxµm diameter, ~1mm length**
- **The assembly is done by xxx in xxx.**
- **The packaging cost is estimated to $xx per component.**
- **The packaging yield is estimated to range from xx% to xx%.**

Package Assembly process flow

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