

# SEOUL Semiconductor – Z-Power P9 LED

## Reverse Costing Analysis

by System Plus Consulting & MuAnalysis

- Analyze the cost of projects at the R&D level
- Enhance the negotiation power of purchasing managers
- Benchmark competitor's products

System Plus Consulting is proud to publish the reverse costing report of the Z-Power P9 LED supplied by SEOUL Semiconductor. Based on a complete teardown process performed by MuAnalysis, the report provides an estimation of the production cost as well as the selling price of the component.

The Z-Power LED P9 series is round type and consumes 0.5 watt at 150mA. It features a diameter of 5mm and the average brightness is 25 lm. The component is provided in a specific 2-pins package, compatible with SMT process.

It is used in various applications such as automotive lighting, large size LCD backlight, mobile phone flash.

**This report provides complete teardown and cost estimation of the component with :**

- Detailed photos
- Material analysis
- Schematic assembly description
- Manufacturing Process Flow
- In-depth economical analysis
- Manufacturing cost breakdown
- Selling price estimation



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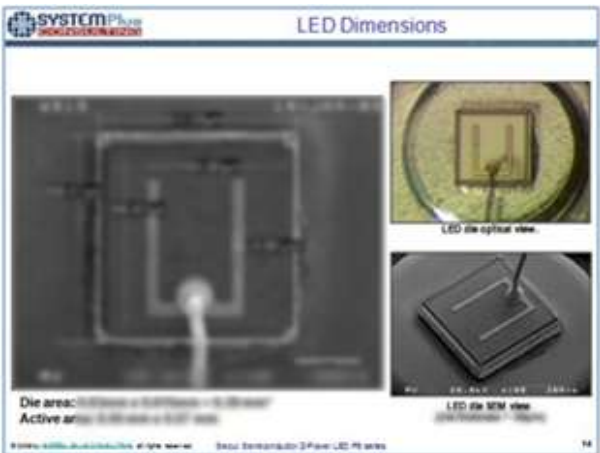
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**LED Die Process Flow**

The LED is manufactured by Seoul Semiconductor in the 100mm foundry located in Ansan, South Korea.

Based on the previous technical observations, we have modeled the process flow with our Cost Simulation Tool "LED Co Sim+ v1.0" which has been developed to simulate the manufacturing process of any type of LED.

The Cost Simulation Tool "LED Co Sim+ v1.0" developed by System Plus Consulting.

**LED Wafer Cost**

Category	Cost	Yield	Unit Cost	Cost	Yield	Unit Cost
Substrate Cost	0.1000	0.75%	0.1333	0.1000	0.75%	0.1333
Manufacturing Cost	0.1000	0.75%	0.1333	0.1000	0.75%	0.1333
Wafer Cost	0.2000	0.75%	0.2667	0.2000	0.75%	0.2667
Probe Cost	0.0000	0.00%	0.0000	0.0000	0.00%	0.0000
<b>TOTAL</b>	<b>0.2000</b>	<b>0.75%</b>	<b>0.2667</b>	<b>0.2000</b>	<b>0.75%</b>	<b>0.2667</b>

**Wafer cost breakdown (per unit wafer)**

- The main part of the wafer cost is due to the "Wafer Losses (20%) in the "Medium Yield" version. This low yield is due to the Epitaxy step which seems to be very complicated to produce.
- The Raw Wafer cost is \$100 (20%) for a 100mm (4-in) wafer.
- This Raw Wafer cost could be reduced if the wafer is reused to produce other dies. By this way, the cost should be divided by the number of reuses and a surface treatment cost should be added. But according to our information, it is often cheaper to use a new one.

**Packaging Cost Details**

Category	Cost	Yield	Unit Cost
Equipment/Process Cost	0.00	0.00%	0.00
Raw Material	0.00	0.00%	0.00
Wafer Cost	0.00	0.00%	0.00
Probe Cost	0.00	0.00%	0.00
Assembly Cost	0.00	0.00%	0.00
Final Test Cost	0.00	0.00%	0.00
<b>TOTAL</b>	<b>0.00</b>	<b>0.00%</b>	<b>0.00</b>

The total packaging cost is estimated to:

- The cost by step includes the equipment cost, the material cost and the labor cost.
- The processor part is high with 42%.

**Packaging Step Cost Breakdown**

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