

EWLP from Casio Micronics

WL-CSP 309-pin Reverse Costing Analysis

by System Plus Consulting

Reverse Analysis Report of the world record Fan-In Wafer Level Package realization featuring 309 pins at a pitch of 0.4mm!

System Plus Consulting is proud to publish the reverse costing report of the last **Wafer Level Chip scale Package** of Casio Micronics, the EWLP. It's used in the Fujitsu MB39C311A, a Power Management Unit + Audio Interface Unit IC for mobile phone.

This EWLP is the last generation of WL-CSP. All the packaging operations are done at the wafer level. The ball pitch is only 0.4mm and only one redistribution layer is used for the 309 balls on 7.45x7.45 mm package.

This WL-CSP with a pitch of 0.4mm is manufactured on 200mm wafers by Casio Micronics.

This report provides a complete teardown of the Casio Micronics 0.4mm pitch WL-CSP package including:

- Detailed photos
- Material analysis
- Manufacturing Process Flow
- In-depth economical analysis
- Manufacturing cost breakdown
- Selling price estimation

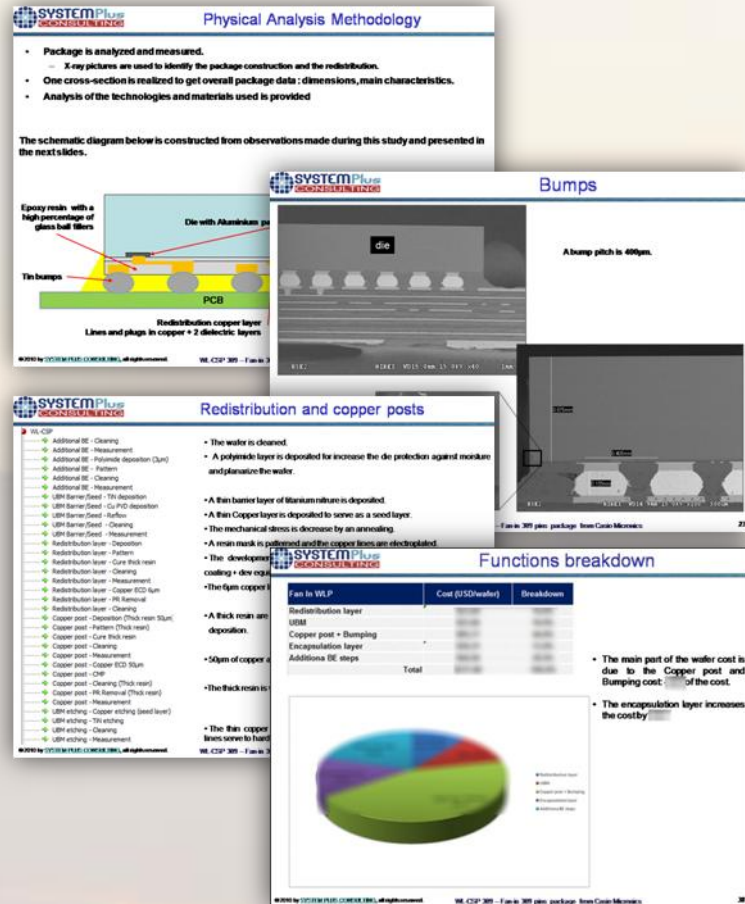


TABLE OF CONTENTS

<p>Overview / Introduction p4</p> <ul style="list-style-type: none"> • Executive Summary • Reverse Costing Methodology 	<p>Manufacturing Process Flow p28</p> <ul style="list-style-type: none"> • The Process flow main steps • WL-CSP Process Flow • Redistribution and copper post • Bumping and Dicing
<p>Fan-In package Principle p7</p> <ul style="list-style-type: none"> • Benefits of WL-CSP • WL-CSP – Reconstitution Flow 	<p>Cost Analysis p35</p> <ul style="list-style-type: none"> • Assumptions • Package Yields • WL-CSP Wafer Cost • Wafer Cost per Equipment Family • Wafer Cost per Consumable Family • WL-CSP Package Cost • Synthesis of the Cost Analysis
<p>Physical Analysis p12</p> <ul style="list-style-type: none"> • Physical Analysis Methodology • Mobile Phone & PCB • MB39C311A circuit • Underfill • Die in the package • Pads and the redistribution layer • Aluminum pad • Coupling layer • Die metallization and passivation • Bumping process • Copper posts • Summary of Physical Data 	<p>Estimated Manufacturer Price Analysis p45</p> <ul style="list-style-type: none"> • Price definitions • Manufacturers financial ratios • Estimated manufacturer Price <p>Conclusion p49</p>

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