

Texas Instruments DLP® - MEMS DMD

Reverse Costing Analysis

by System Plus Consulting

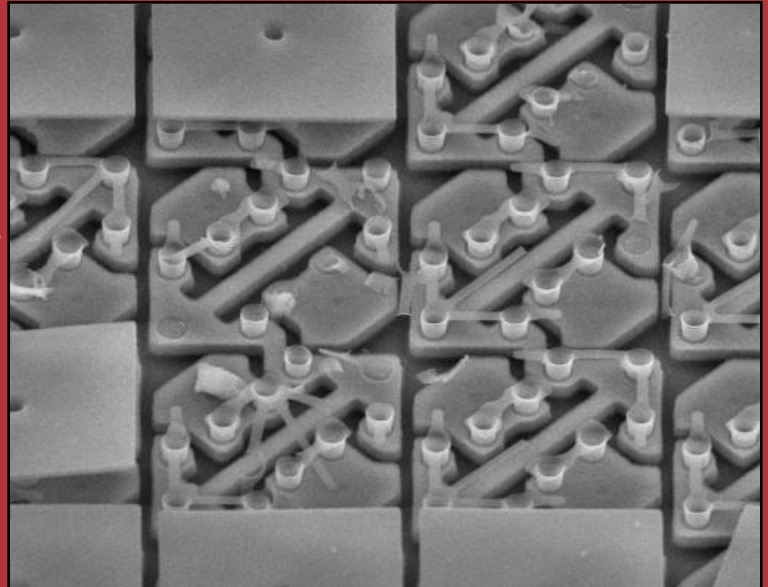
- **Analyze the cost of projects at the R&D level**
- **Enhance the negotiation power of purchasing managers**
- **Benchmark competitor's products**

System Plus Consulting is proud to publish the reverse costing report of the MEMS Digital Micromirror Device (DMD) for pico-projectors supplied by Texas Instruments. Based on a complete reverse engineering process the report provides an estimation of the production cost as well as the selling price of the circuit.

This Texas Instruments DLP® component is used in pico-projectors systems which can be integrated in phones or in pocket projectors. It uses a specific MEMS technology process using around 187K micromirrors with a 7x7µm area to perform a picture. The micromirrors are combined with a CMOS integrated circuit and SRAM memory for the control. The device uses a wafer level packaging technology and a ceramic substrate.

This report provides complete teardown of the MEMS with :

- **Detailed photos**
- **Material analysis**
- **Schematic assembly description**
- **Manufacturing Process Flow**
- **In-depth economical analysis**
- **Manufacturing cost breakdown**
- **Selling price estimation**

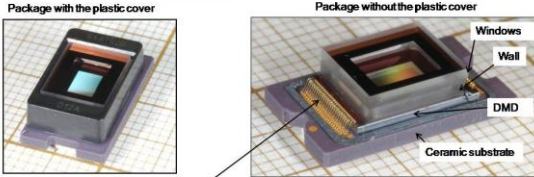


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Package



Package with the plastic cover

Package without the plastic cover

96 Wire bondings

Windows

Wall

DMD

Ceramic substrate

Piece of glass called Windows 8 x 6.9 x 1mm

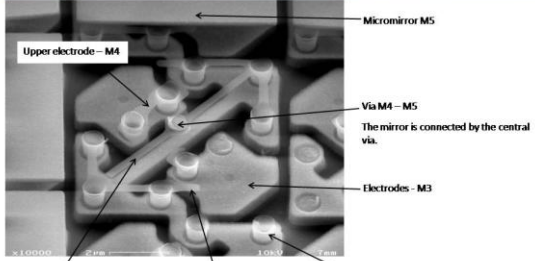
Piece of glass called Wall 8 x 6.9 x 1mm

DMD 10 x 7 x 0.72mm

Ceramic Substrate 16 x 9 x 1.2mm

Connector board to board 46 pins

Micromirror - Pictures



Micromirror M5

Upper electrode - M4

Via M4 - M5
The mirror is connected by the central via.

Electrodes - M3

Via M3 - M4

Torsion Hinge - M4
The torsion hinges are very thin.

Spring tips - M4
The spring optimizes the

Back End Process Flow

A thin anti-striktion layer of silicon is deposited, passivation.

The wafer is temporarily bonded on adhesive tape for the test.

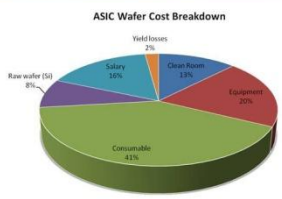
The windows are placed and glued on the DMD.

- Bonding Adhesive
- Test Optical and Electrical
- Debonding Adhesive
- Plasma cleaning
- Passivation
- Pick and place Wall
- Pick and place window
- Cure
- Wafer break

- Glass wall
 - milling opening
 - Cleaning
 - Saw
 - Cleaning
 - Dispenser adhesive
- Glass window
 - Deposit Chrome
 - Pattern
 - Etching Chrome
 - PR removal
 - Saw

ASIC Wafer Cost

	Cost	Breakdown
Clean Room		16.3%
Equipment		26.2%
Consumable		53.9%
Raw wafer (Si)		11.0%
Salary		21.6%
Yield losses		2.8%
TOTAL		



ASIC Wafer Cost Breakdown

- Standard CMOS process cost.
- The wafer cost does not decrease between 2009 and 2010.
- The main part of the wafer cost is due to the consumables.
- The salary part is high (16%) because the location of the wafer fabrication unit is North America.
- The manufacturing yield is around 98%, from 2009 to 2010. The mature technology explains this correct value of manufacturing yield. (The average value for industry)

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System Plus Consulting performs reverse costing analyses of

- Integrated circuits Electronic boards
- MEMS Electronic systems
- System In Package (SiP) Smartcards

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